PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Book IC16 1986

C MOS integrated circuits for clocks and watches

Elcoma – Philips Electronic Components and Materials Division – embraces a world-wide group of companies operating under the following names:

IBRAPE
RTC
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Elcoma offers you a technological partnership in developing your systems to the full. A partnership to which we can bring

- world-wide production and marketing
- know-how
- systems approach
- continuity
- broad product line
- fundamental research
- leading technologies
- applications support
- quality

CMOS INTEGRATED CIRCUITS FOR CLOCKS AND WATCHES

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons**

T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T8 **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers and infrared detectors**

T15 **Dry reed switches**

T16 **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8a **Light-emitting diodes**

S8b **Devices for optoelectronics**
Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

S11 **Microwave transistors**

S12 **Surface acoustic wave devices**

S13 **Semiconductor sensors**

INTEGRATED CIRCUITS (PURPLE SERIES)

The NEW SERIES of handbooks is now completed. With effect from the publication date of this handbook the "N" in the handbook code number will be deleted.
Handbooks to be replaced during 1986 are shown below.

The purple series of handbooks comprises:

IC01	**Radio, audio and associated systems** Bipolar, MOS	new issue 1986 IC01N 1985
IC02a/b	**Video and associated systems** Bipolar, MOS	new issue 1986 IC02Na/b 1985
IC03	**Integrated circuits for telephony** Bipolar, MOS	new issue 1986 IC03N 1985
IC04	**HE4000B logic family** CMOS	new issue 1986 IC4 1983
IC05N	**HE4000B logic family — uncased ICs** CMOS	published 1984
IC06N	**High-speed CMOS; PC74HC/HCT/HCU** Logic family	published 1986
IC08	**ECL 10K and 100K logic families**	New issue 1986 IC08N 1984
IC09N	**TTL logic series**	published 1986
IC10	**Memories** MOS, TTL, ECL	new issue 1986 IC7 1982
IC11N	**Linear LSI**	published 1985
Supplement to IC11N	**Linear LSI**	published 1986
IC12	**I^2C-bus compatible ICs**	not yet issued
IC13	**Semi-custom** Programmable Logic Devices (PLD)	new issue 1986 IC13N 1985
IC14N	**Microprocessors, microcontrollers and peripherals** Bipolar, MOS	published 1985
IC15	**FAST TTL logic series**	new issue 1986 IC15N 1985
IC16	**CMOS integrated circuits for clocks and watches**	first issue 1986
IC17	**Integrated Services Digital Networks (ISDN)**	not yet issued
IC18	**Microprocessors and peripherals**	new issue 1986*

* The Microprocessors were included in handbook IC14N 1985, so IC18 will replace that part of IC14N.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

INTRODUCTION

INTRODUCTION

Faselec, a Philips IC subsidary, is one of the most important producers of CMOS integrated circuits for clocks and watches in the world. Situated in Switzerland, the heart of the European clock and watch industry, Faselec benefits to a large degree from this unique industrial environment. It is therefore not surprising, that Faselec was one of the first semiconductor companies to apply the silicon gate CMOS (complementary metal oxide semiconductor) technology in the production of clock and watch circuits and was the first company to offer an SO package (mini-pack) back in the seventies.

Facelec maintains its position at the forefront of the clock and watch IC industry, being the first company to offer the EEPROMs (Electrically Erasable Programmable Read Only Memories), with operating voltages as low as 1,1 V, for frequency adjustment. This latest development enables the industry to find better technical and cost effective solutions for their products.

To enable the clock and watch industry to maintain its world-renowned quality image, Faselec has implemented a Company-Wide Quality Improvement (CWQI) program. This CWQI program, involving every employee of Faselec, features a continuous improvement of customer service and product quality. This commitment to quality has lead to us being able to set our standard at zero defects and now enables us to offer our customers a zero defects warranty. The warranty means that if he finds a single device which does not conform to the published specification, the customer can return the complete lot for rescreening or replacement. Faselec is the first company in the world to offer the clock and watch industry a zero defects warranty.

At Faselec quality is something that dominates all phases of manufacture. Quality is built into the product by the conscious use of advanced technological aids and a continuous monitoring of all process steps through in-line quality controls. Additionally a stringent incoming inspection of all materials used assures an end-product with an inherently high quality level.

All products are 100% tested against published specifications, any device not conforming to the specifications is rejected. Conformity of each lot to the published specifications is double-checked by our Quality department, which is independent from production.

The dedication of the highly-qualified personnel and the large amount of know-how accumulated over the years, backed by constant efforts in developing new process and packaging technology as well as new products, makes Faselec the preferred source for your clock and watch circuits.

SELECTION GUIDE

FUNCTIONAL INDEX

Analogue watch circuits: 32 kHz

type number	output cycle time	pulse duration	current consumption		EEPROM	comments
			typ.	max.		
PCA1201	1 s	7,8 ms	150 nA	200 nA	no	C_i = 3,5 pF for the PCA1200 series except PCA1212
PCA1203	20 s	7,8 ms	150 nA	200 nA	no	
PCA1204	5 s	7,8 ms	150 nA	200 nA	no	
PCA1205	12 s	6,8 ms	150 nA	200 nA	no	
PCA1207	10 s	7,8 ms	150 nA	200 nA	no	
PCA1209	1 s	5,9 ms	150 nA	200 nA	no	
PCA1212	1 s	7,8 ms	150 nA	200 nA	no	C_i = 16 pF
PCA1243	20 s	6,8 ms	150 nA	200 nA	no	
PCA1246	1 s	3,9 ms	150 nA	200 nA	no	
PCA1247	1 s	6,8 ms	150 nA	200 nA	no	
PCA1248	10 s	5,9 ms	150 nA	200 nA	no	
PCA1249	12 s	5,9 ms	150 nA	200 nA	no	
PCA1260	1 s	7,8 ms	150 nA	250 nA	no	end-of-life battery detector and adaptive motor control
PCA1261	1 s	7,8 ms	150 nA	250 nA	no	adaptive motor control without end-of-life detector
PCA1401	1 s	7,8 ms	200 nA	300 nA	yes	PCA1400 series have: EEPROM for frequency trimming, adjustment accuracy ± 2×10^{-6} (except PCA1408 and PCA1411)
PCA1403	20 s	7,8 ms	200 nA	300 nA	yes	
PCA1404	5 s	7,8 ms	200 nA	300 nA	yes	
PCA1408	20 s	5,8 ms	200 nA	300 nA	no	no adjustment

Analogue watch circuits: 32 kHz

type number	output cycle time	pulse duration	current consumption		EEPROM	comments
			typ.	max.		
PCA1409	1 s	5,8 ms	200 nA	300 nA	yes	PCA1400 series have: EEPROM for frequency trimming, adjustment accuracy ± 2 x 10^{-6} (except PCA1408 and PCA1411)
PCA1411	1 s	7,8 ms	200 nA	300 nA	no	no adjustment
PCA1412	1 s	31,2 ms	200 nA	300 nA	yes	
PCA1426	20 s	5,8 ms	200 nA	300 nA	yes	
PCA1446	1 s	3,9 ms	200 nA	300 nA	yes	
PCA1449	12 s	5,8 ms	200 nA	300 nA	yes	
PCA1460	1 s	7,8 ms	170 nA	260 nA	yes	PCA1460 series have: EEPROM for frequency trimming, adjustment accuracy ± 2,5 x 10^{-6}; Detector for silver oxide (end-of-life), except PCA1461, and lithium battery voltage levels; All types have adaptive motor control
PCA1461	1 s	7,8 ms	170 nA	260 nA	yes	
PCA1462	1 s	5,8 ms	170 nA	260 nA	yes	
PCA1463	1 s	3,9 ms	170 nA	260 nA	yes	

Analogue alarm clock circuits: 32 kHz quartz crystal

type number	output cycle time	pulse duration	current consumption		EEPROM	comments
			typ.	max.		
PCA1584	1 s	46,8 ms	1,5 μA	5 μA	yes	EEPROM for frequency trimming; 64 steps 2 kHz alarm output. See Fig. 1.
PCA1585	1 s	46,8 ms	1,5 μA	5 μA	yes	EEPROM for frequency trimming; 64 steps 2 kHz alarm output. See Fig. 2.
PCA1586	1 s	15,6 ms	1,5 μA	5 μA	yes	EEPROM for frequency trimming; 64 steps 2 kHz alarm output. See Fig. 1.
PCA1587	4 s	15,6 ms	1,5 μA	5 μA	yes	EEPROM for frequency trimming; 64 steps 2 kHz alarm output. See Fig. 2.

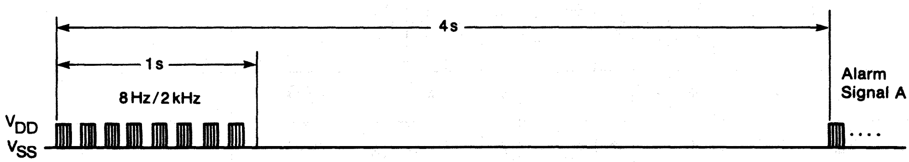


Fig. 1 Alarm output diagram A.

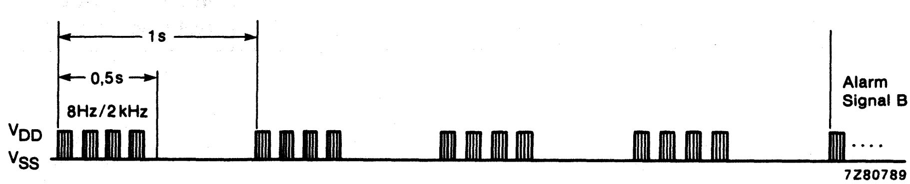


Fig. 2 Alarm output diagram B.

Analogue alarm clock circuit: 4,19 MHz quartz crystal

type number	output cycle time	pulse duration	current consumption typ.	current consumption max.	EEPROM	comments
PCA1512	1 s	1 s	25 μA	45 μA	no	alarm output for d.c. buzzer
PCA1517	1 s	46,8 ms	25 μA	45 μA	no	alarm output for external n-p-n transistor

Digital car clock circuits: 4,19 MHz quartz crystal

type number	digits	functions: 12 hours mode	24 hours mode	AM/PM annunciator	hours	minutes	direct drive	duplex drive	internal voltage regulator	EEPROM	typical supply current μA	comments
PCF1171	4	●	●		●	●	●		●		400	
PCF1172	3,5	●		●	●	●	●		●		400	
PCF1174	4	●	●	●	●	●	●		●	●	700 to 1000	EEPROM for frequency trimming and internal voltage regulation for LCD
PCF1175	4	●	●	●	●	●		●	●	●	700 to 1000	EEPROM for frequency trimming and internal voltage regulation for LCD

NUMERICAL INDEX

TYPE DESIGNATION

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : –55 to + 125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

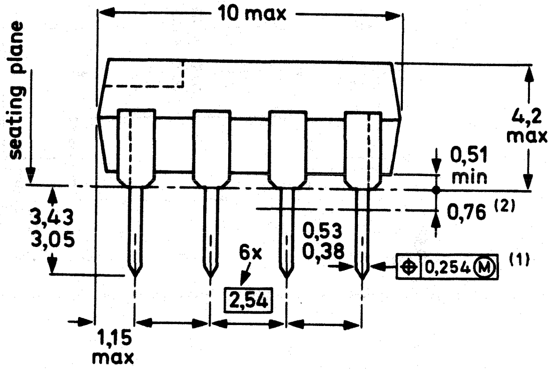
To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

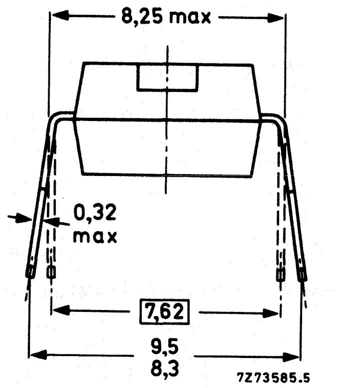
Voltage surges

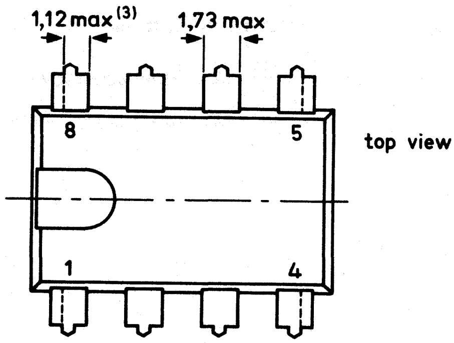
Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

PACKAGE OUTLINES

8-LEAD DUAL IN-LINE; PLASTIC (SOT-97A)







Dimensions in mm

⊕ Positional accuracy.

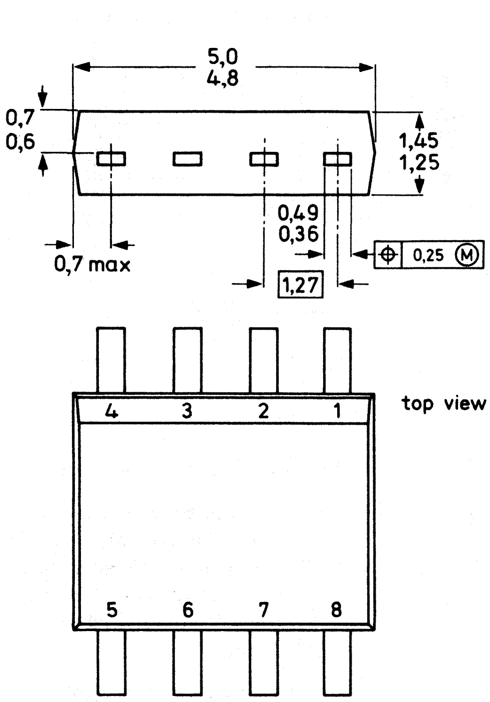
Ⓜ Maximum Material Condition.

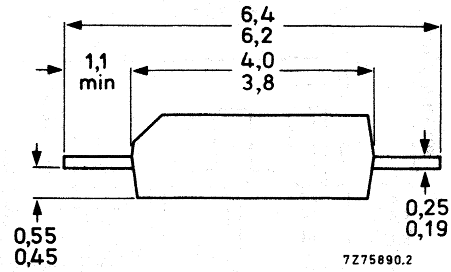
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

8-LEAD MINI-PACK; PLASTIC (SO-8; SOT-96C)



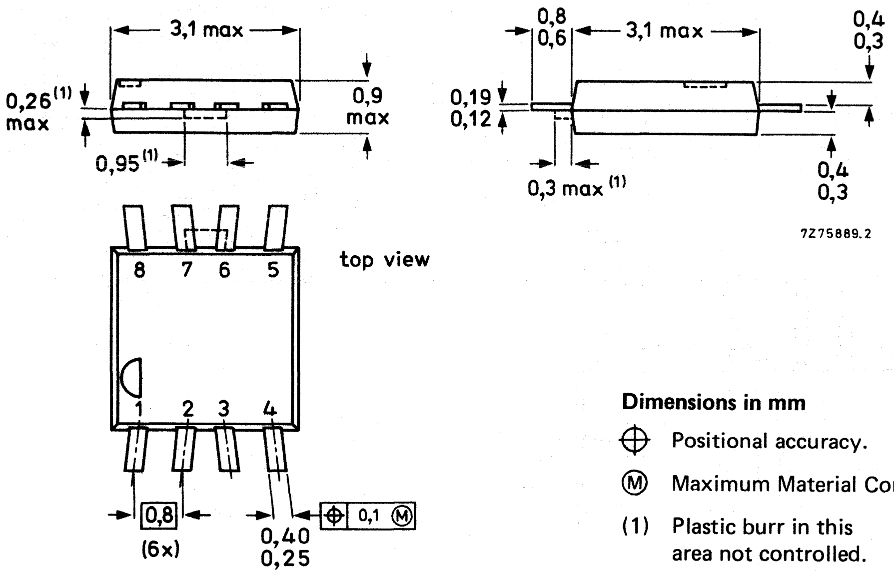


Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

8-LEAD MICRO-FLAT-PACK; PLASTIC (SOT-144)



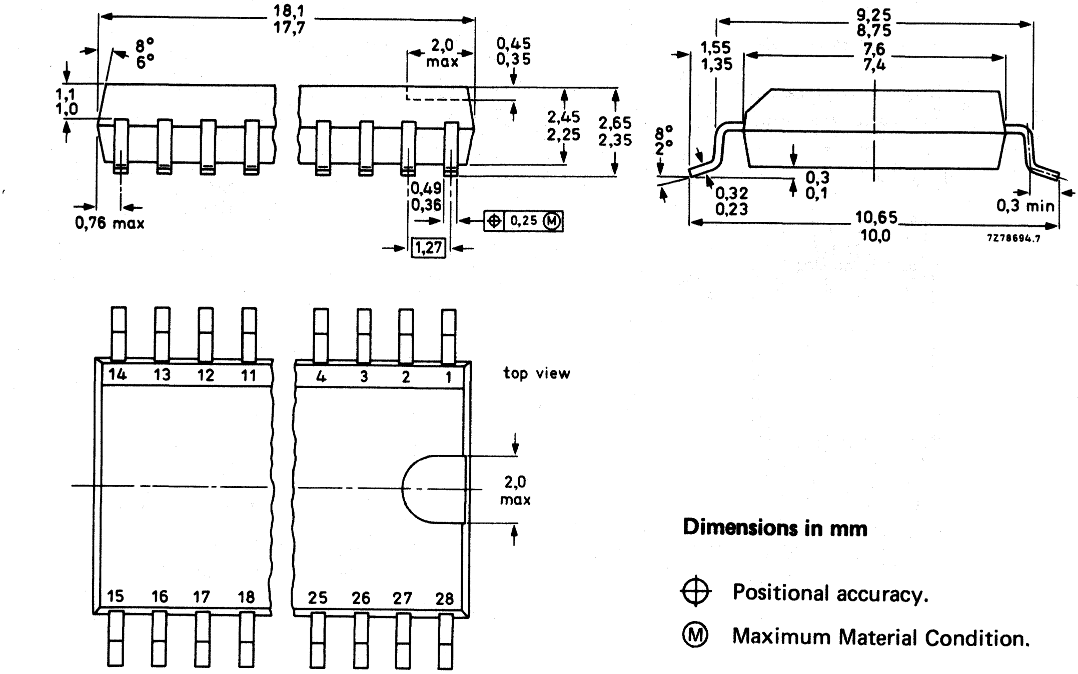
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Plastic burr in this area not controlled.

28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)

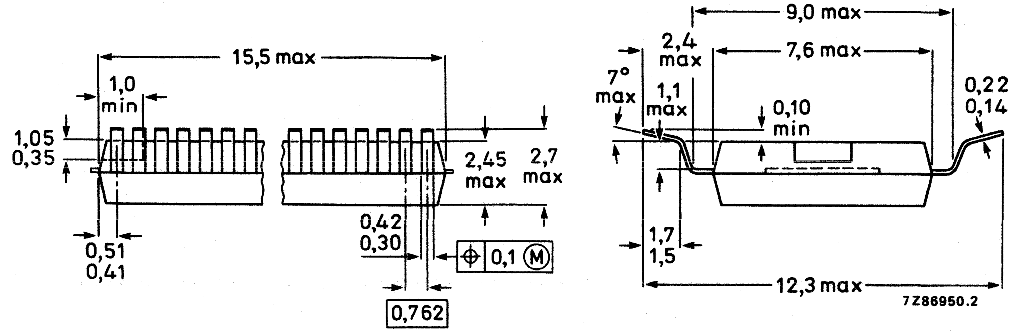


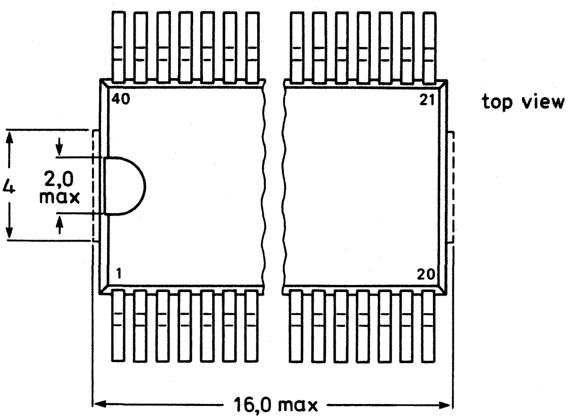
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

40-LEAD MINI-PACK; PLASTIC (OPPOSITE BENT LEADS) (VSO-40; SOT-158B)





Dimensions in mm

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING INFORMATION

SOLDERING INFORMATION

FOR MINI-PACK; PLASTIC:

(SO-8, SOT-96C)
(SO-28, SOT-136A)
(VSO-40, SOT-158B)

1. **By hand-held soldering iron or pulse-heated solder tool**

   Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

   For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. **By wave**

   Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

   A modified wave soldering technique is recommended, using two solder waves (dual-wave); a first turbulent wave with high upward pressure is followed by a smooth, laminar wave. A mildly activated flux will eliminate the need for removal of corrosive residues in most applications.

3. **By solder paste reflow**

   Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing or pressure-syringe dispensing before device placement.

   Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 8 and 60 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

   Pre-heating is necessary to dry paste and evaporate binding agent, and to reduce thermal shock on entry to reflow zone.

4. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.

FOR MICRO-FLAT-PACK; PLASTIC:

(SOT-144)

1. Reflow soldering

Reflow soldering by means of pulse-heating or infrared ovens can be applied. Precautions should be taken to hold the temperatures of the integrated circuit body and the printed-circuit board low.

General limits

IC-body max. 300 ^{o}C – 5 s
average PC-board max. 150 ^{o}C

Indications

Pulse-heating: 350 ^{o}C – 2 s
Infrared heater: short-wave heaters, high speed and low power

FOR DUAL-IN-LINE; PLASTIC

(SOT-97A)

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 ^{o}C it must not be in contact for more than 10 seconds; if between 300 ^{o}C and 400 ^{o}C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 ^{o}C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

DEVICE DATA

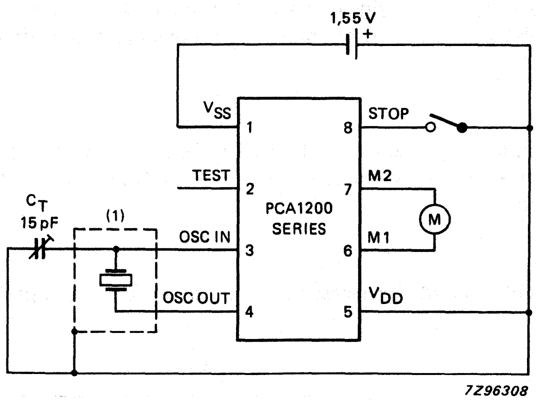
32 kHz WATCH CIRCUIT FOR BIPOLAR MOTORS

GENERAL DESCRIPTION

The PCA1200 is a CMOS integrated circuit specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with bipolar stepping motors.

Features

- 32 kHz oscillator, with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Low current consumption: typically 150 nA
- Output for bipolar stepping motor
- Stop function for accurate timing
- Test mode with 32 Hz motor output frequency for testing the mechanical parts of the watch
- Output cycle time and pulse duration can be adjusted to specific customer applications with the interconnection mask



(1) Case to be connected to V_{DD}.

Fig. 1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA12XXT: 8-lead micro-flat-pack; plastic (SOT-144).
PCA12XXU: chip in tray.

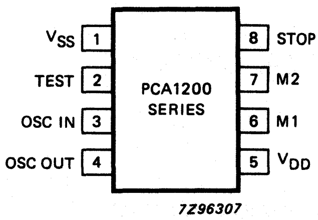


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	supply voltage
6	M1	motor 1 output
7	M2	motor 2 output
8	STOP	motor stop

FUNCTIONAL DESCRIPTION AND TESTING

Normal mode

"STOP" : (pin 8) open
"TEST" : (pin 2) open

Stop mode

The motor is stopped by connecting "STOP" (pin 8) to V_{DD}. The STOP input operates after 7 to 16 ms to prevent an accidental motor stop by shock or contact bounce. A motor pulse which has already started cannot be affected by a signal on the STOP input. The first motor pulse will appear with reversed polarity (relative to the previous motor pulse) one cycle time after disconnecting the stop signal.

Test mode 1 (motor test)

"TEST" (pin 2) connected to V_{DD}. Switch-on delay: 7 to 16 ms. In this mode a 32 Hz signal appears on the motor outputs. For all types the motor output period is 31,25 ms and the pulse width is the same as in the normal mode.

Test mode 2 (IC test)

"TEST" (pin 2) and "STOP" (pin 8) connected to V_{DD}. For motor output periods and the pulse widths, see Table 1.

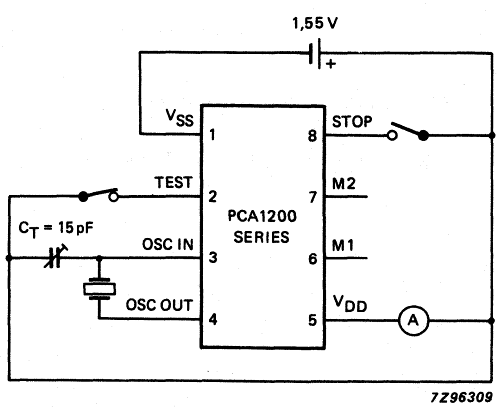


Fig. 3 Test circuit for test mode 1 (pin 2 connected to V_{DD}).

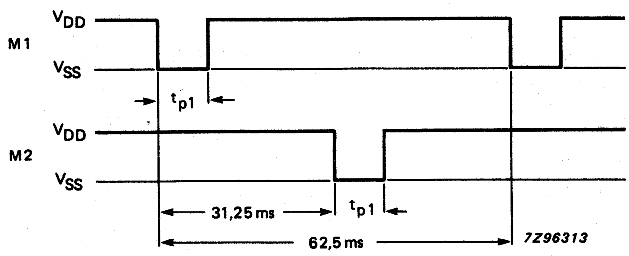


Fig. 4 Motor output waveforms in motor test mode 1.

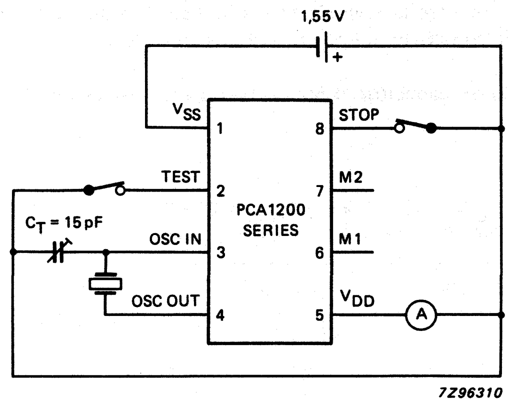


Fig. 5 Test circuit for test mode 2 (pins 2 and 8 connected to V_{DD}).

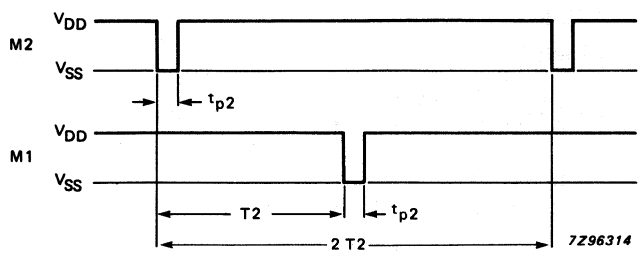


Fig. 6 Motor output waveforms in motor test mode 2.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1,8 to + 5 V
All input voltages; note 2	V_I	V_{SS} to V_{DD} V
Output short-circuit duration		indefinite
Operating ambient temperature range	T_{amb}	−10 to + 60 °C
Storage temperature range	T_{stg}	−30 to + 100 °C
Resistance against electrostatic discharges		note 3

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').
3. Three discharges of a 100 pF capacitor at 800 V, through a resistor of 1,5 kΩ (with positive and negative polarity).

CHARACTERISTICS

V_{DD} = 1,55 V; V_{SS} = 0 V; f_{osc} = 32,768 kHz; T_{amb} = 25 °C; crystal: f = 32 kHz; C_L = 8 to 10 pF; C_1 = 2 to 3 fF; C_o = 1 to 3 pF; R_s = 15 kΩ (typical) and 40 kΩ (max.) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	1,2	1,55	1,8	V
Supply voltage	transient V_{DD} = 1,55 V	ΔV_{DD}	–	–	0,25	V
Supply current	$R_M = \infty$ R_s = 15 kΩ	I_{DD}	–	150	200	nA
Motor outputs						
Cycle time	Table 1	T	1	–	30	s
Pulse width	Table 1	t_p	1	–	14	ms
Sum of saturation voltages	R_M = 2 kΩ	ΣV_{sat}	–	80	150	mV
Output short-circuit impedance	between motor pulses	R_{os}	–	100	200	Ω
Oscillator						
Starting voltage		$V_{OSC\ ST}$	1,2	1,1	–	V
Transconductance	$V_{i(p-p)}$	g_m	4	8	–	µS
Start-up time		t_{OSC}	–	1	5	s
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	$0,1 \times 10^{-6}$	$0,3 \times 10^{-6}$	
Frequency tolerance	note 1 C_1 = 2,5 fF	Δf/f	–	$\pm 3 \times 10^{-6}$	$\pm 10 \times 10^{-6}$	

parameter	conditions	symbol	min.	typ.	max.	unit
Input capacitance	note 2	C_i	–	3,5	–	pF
Output capacitance	$V_{i(p-p)}$	C_o	–	24	–	pF
Motor stop						
Peak input current	7,8 to 0,244 ms	I_{im}	–	1	–	μA
Average input current	duty factor 1 : 32	$I_{i(av)}$	–	30	–	nA
Stop delay		t_{dSTOP}	7	–	16	ms
Test input						
Peak input current	7,8 to 0,244 ms	I_{im}	–	1	–	μA
Average input current	duty factor 1 : 32	$I_{i(av)}$	–	30	–	nA
Test delay		t_{dTEST}	7	–	16	ms

Notes to the characteristics

1. Frequency tolerance device-to-device C_L = 10 pF.
2. Input capacitance measured on the 8-lead micro-flat-pack (SOT-144).

DEVELOPMENT DATA

Table 1 Available types

type no.	cycle time T (s)	pulse duration t_p (ms)	test mode 1 $T1/t_{p1}$ (ms)	test mode 2 $T2/t_{p2}$ (ms)	C_i (pF)
PCA1201	1	7,8	31,25 7,8	62,5 0,977	3,5
PCA1203	20	7,8	31,25 7,8	312,5 0,244	3,5
PCA1204	5	7,8	31,25 7,8	78,1 0,244	3,5
PCA1205	12	6,8	31,25 7,8	187,5 0,244	3,5
PCA1207	10	7,8	31,25 7,8	156,25 0,244	3,5
PCA1209	1	5,9	31,25 5,9	62,5 0,977	3,5
PCA1212	1	7,8	31,25 7,8	62,5 0,977	16
PCA1243	20	6,8	31,25 6,8	312,5 0,244	3,5
PCA1246	1	3,9	31,25 3,9	62,5 0,977	3,5
PCA1247	1	6,8	31,25 6,8	62,5 0,977	3,5
PCA1248	10	5,9	31,25 5,9	156,25 0,244	3,5
PCA1249	12	5,9	31,25 5,9	187,5 0,244	3,5

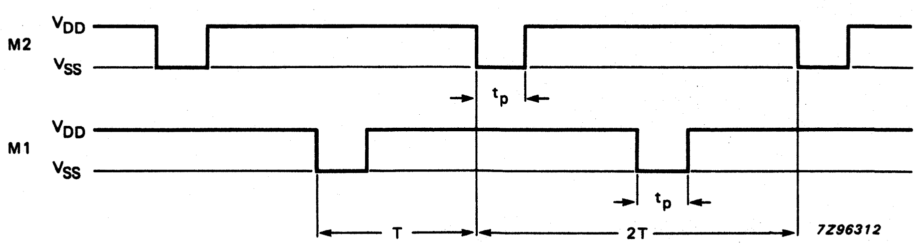


Fig. 7 Motor output waveforms normal mode.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

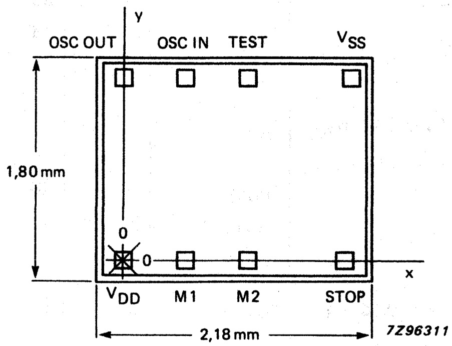


Fig. 8 Bonding pad locations.

Bonding pad dimensions 120 μm x 120 μm
Chip area = 3,9240 mm^2

Table 2 Bonding pad locations (dimensions in μm)

All x, y co-ordinates are referenced to the bottom left pad (V_{DD}), see Fig. 8.

pad	x	y
V_{SS}	1820	1470
TEST	1000	1470
OSC IN	500	1470
OSC OUT	0	1470
V_{DD}	0	0
M1	500	0
M2	1000	0
STOP	1760	0
chip corner max. value	−160	−160

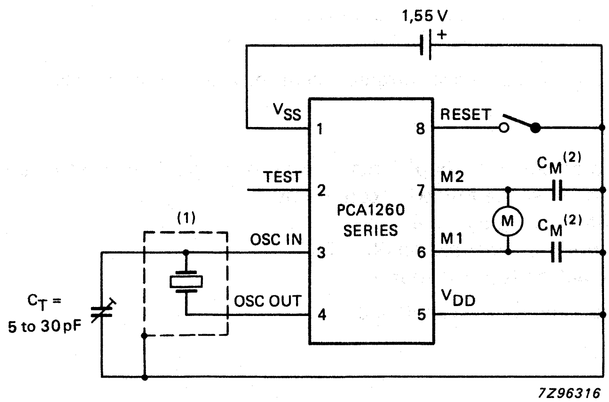
32kHz WATCH CIRCUIT WITH ADAPTIVE MOTOR PULSE WIDTH FOR BIPOLAR MOTORS

GENERAL DESCRIPTION

The PCA1260 is a CMOS integrated circuit specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with bipolar stepping motors.

Features

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Oscillator output capacitor is integrated, only crystal and trimmer required as external components
- Very low current consumption: typically 160 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current, compared with conventional circuits, by self adaption of the motor pulse width according to the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Stop function for accurate timing
- Various test modes for testing the mechanical parts of the watch as well as the IC itself
- Two available types: PCA1260 and PCA1261



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0,5 pF or larger than 100 MΩ.

(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} should be less than C_M = 80 pF for correct operation of the detection circuit.

Fig. 1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA1260/61T: 8-lead micro-flat-pack; plastic (SOT-144).
PCA1260/61U: chip in tray.

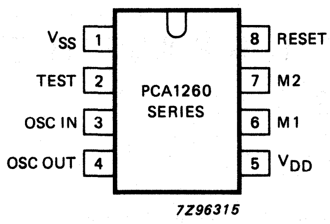


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	supply voltage
6	M1	motor 1 output
7	M2	motor 2 output
8	RESET	reset input

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different widths depending on the torque required to turn the motor (Fig. 4). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. If a step is missed a correction sequence will be started (Fig. 3).

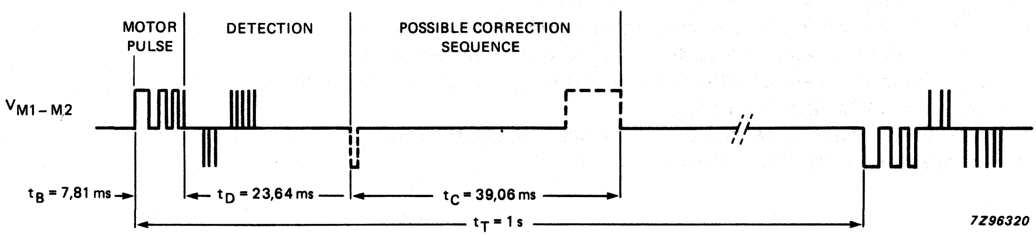


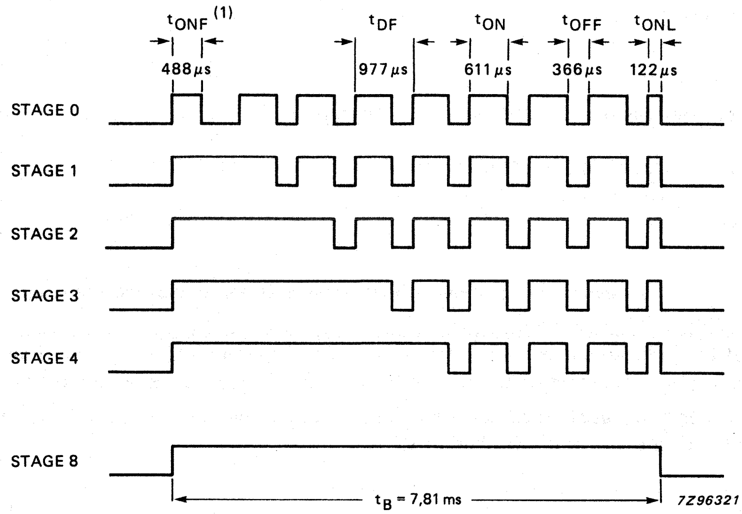
Fig. 3 Typical motor output waveform with motor connected.

Motor pulses

The circuit produces motor pulses of six different widths, or stages. Stages 0 to 4 are used in normal operation, stage 8 occurs under the following conditions:

- correction pulse (after a missing step)
- end-of-life pulses (not implemented on PCA1261)
- if stage 4 is not enough to turn the motor

After a RESET the circuit always starts with a 0.



(1) t_{ONF} for stage 0 to 4 = 488 μs + stage x 977 μs

Fig. 4 Different forms of motor pulses.

DEVELOPMENT DATA

The circuit operates for 64 motor pulses at a fixed stage, if every motor pulse is executed. The next 64 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and the next 63 motor pulses are increased by one stage.

If motor pulses at stage 4 are not large enough, motor pulses of stage 8 will be produced for a maximum of 63 pulses and no attempt will be made to maintain a low current consumption. After this sequence the circuit starts at stage 0 to be stabilized on as low a stage as possible as fast as possible.

Detection of motor pulses

After a motor pulse, the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig. 5 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1 respectively. Then the first of 46 possible measurement cycles (t_{MC}) starts to measure the induced current.

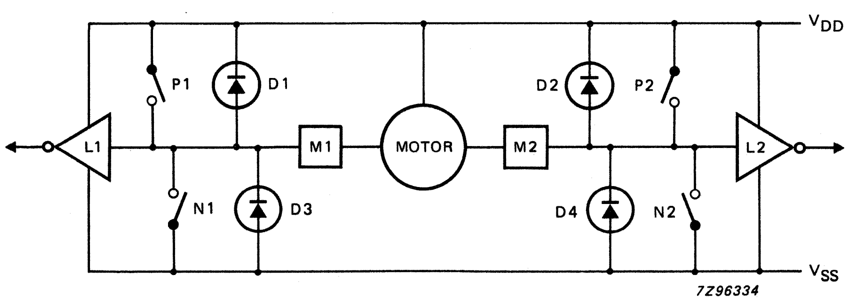


Fig. 5 Motor driving and detecting circuit.

Detection criterion (Figs 6 and 7)

	PCA1260	PCA1261
Part 1		
• number of measured positive current polarities after t_{DI}	P = 3	P = 1
Part 2		
• number of measured positive current polarities since the first negative current polarity is detected after part 1 (see Fig. 7)	N = 5	N = 2
End-of-life cycle	yes	no

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

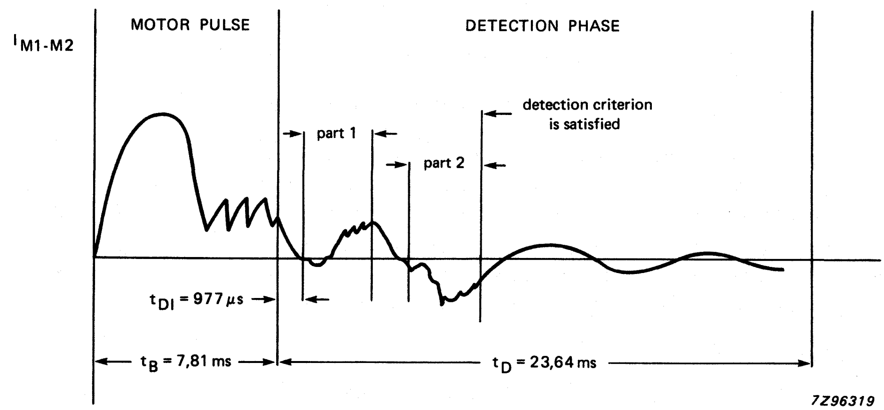


Fig. 6 Typical current waveform of a successfully executed motor pulse.

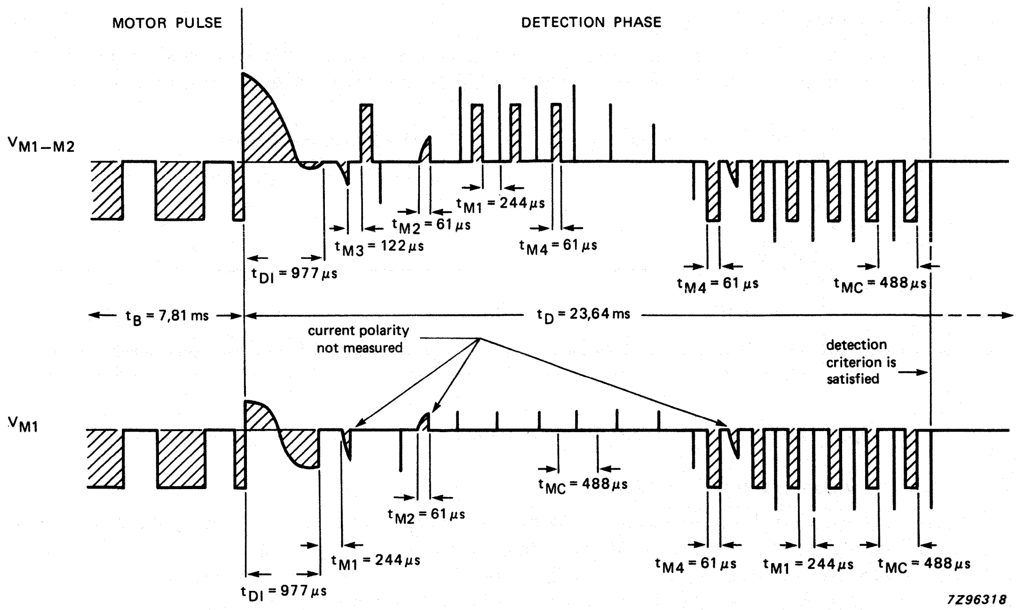


Fig. 7 Detection phase of the current waveform in Fig. 6.

Every measurement cycle (t_{MC}) has 4 phases, they are as follows:

Phase 1: (t_{M1}) During t_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.

Phase 2: (t_{M2}) Measures the induced current. During a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is shorted to V_{DD}. Depending on the direction of the interrupted current flow either:

- the current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2;
- the current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1.

A successfully detected current polarity is normally characterized by a short pulse of 0,5 to 10 µs with a voltage up to ± 2,1 V, failed polarity detection by the maximum pulse width of 61 µs and a voltage of ± 0,5 V (see Fig. 7).

Phase 3: (t_{M3}) The switches P1 and P2 remain closed for the time t_{M3}. If the circuit does not detect the expected polarity, phase 3 is lengthened by the time t_{M4} and phase 4 is omitted.

Phase 4: (t_{M4}) A pulse of time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed.

Detection and pulse width control will be switched off, when battery voltage is below the end-of-life voltage (V_{EOL}) or if stage 4 is not sufficient to turn the motor.

Correction sequence (Fig. 8)

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 31,25 ms a pulse of stage 8 (t_{C2}) to turn the motor.

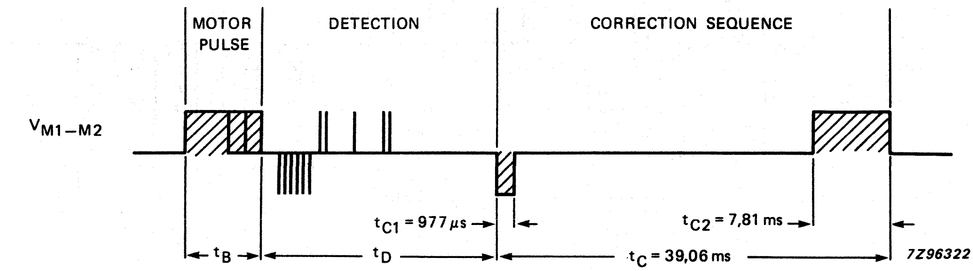


Fig. 8 Correction sequence after a missing motor step with motor connected.

End-of-life (only applicable to PCA1260).

The supply voltage V_{DD} is compared with the internal voltage reference V_{EOL} every 4 s. If the end-of-life of the battery is detected ($V_{DD} > V_{EOL}$), detection and pulse width control will be switched off and the waveforms produced will be of stage 8. In addition the pulses are produced in bursts of 4 pulses every 4 seconds to indicate this condition. After a motor stop the first detection of end-of-life will be made a half a second later.

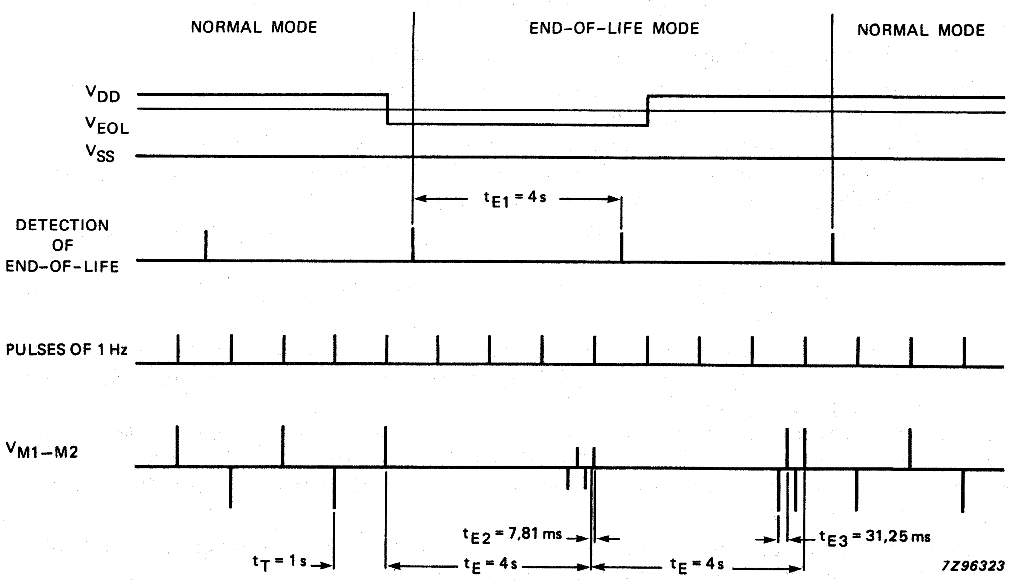


Fig. 9 Motor pulses in end-of-life mode.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for testing and tuning the oscillator.

Connecting the RESET to V_{DD} stops the motor pulses and sets the motor pulse width for the next available motor pulse to stage 0; then, the motor pulses adapt according to the required torque. The RESET input has a built-in delay of 15,7 to 78,1 ms to prevent an accidential motor stop caused by shock or contact bounce. After RESET is activated the first pulse appears with a time delay of 1 s.

Connecting RESET to V_{SS} activates the test mode. With $V_{DD} > V_{EOL}$ motor pulse of stage 8 in a period t_{T1} are produced (Test 1).

If V_{DD} is less than V_{EOL} motor pulses of stage 8 but with a period of t_{T2} are produced (Test 2). In Test 1 and Test 2 the end-of-life detector operates every 7,81 ms.

If V_{DD} is increased again to a voltage higher than V_{EOL}, normal function takes place but the motor pulse period is t_{T3} = 125 ms instead of 1 s (Test 3). In addition the level of the pulse width is reduced every second.

Test and reset mode are terminated by disconnecting the RESET pin.

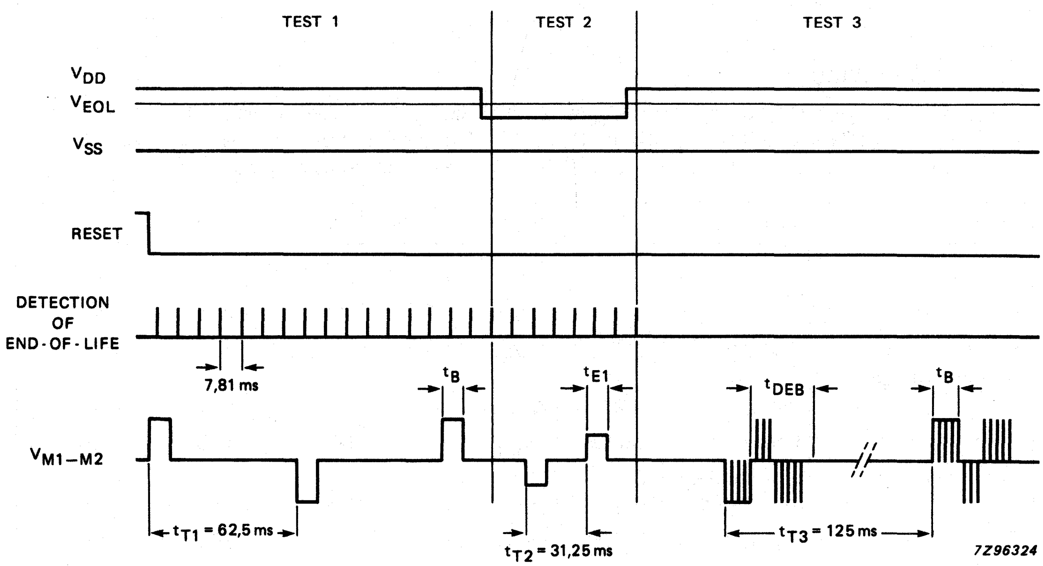


Fig. 10 Output pulses in test modes with RESET at V_{SS}.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1,8 to + 5 V
All input voltages; note 2	V_I	V_{SS} to V_{DD} V
Output short-curcuit duration		indefinite
Operating ambient temperature range	T_{amb}	−10 to + 60 °C
Storage temperature range	T_{stg}	−30 to + 100 °C

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1,55 V; V_{SS} = 0 V; C_T = 12 pF; f_{osc} = 32,768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ typ. and 40 kΩ max.; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_o = 1 to 3 pF; unless otherwise specified
Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD1}	1,2	1,55	2,0	V
Supply voltage	T_{amb} = −10 to + 60 °C	V_{DD2}	1,2	−	1,8	V
Supply voltage	transient within 1,2 V and 2 V	ΔV_{DD}	−	−	0,45	V
Supply current	between motor pulses	I_{DD1}	−	150	250	nA
Supply current	stop mode; pin 8 connected to V_{DD}	I_{DD2}	−	160	280	nA
Supply current	T_{amb} = −10 to + 60 °C	I_{DD3}	−	−	400	nA
Motor output						
Saturation voltage Σ (P + N)	R_M = 2 kΩ	V_{sat}	−	100	150	mV
Saturation voltage Σ (P + N)	R_M = 2 kΩ T_{amb} = −20 to + 60 °C	V_{sat}	−	−	200	mV
Output short-short-circuit impedance	between motor pulses $I_{transistor}$ < 1 mA	R_{os}	−	200	300	Ω

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Starting voltage		$V_{OSC\ ST}$	1,2	–	–	V
Transconductance	$V_{i(p-p)} \leq 50$ mV	g_m	6	15	–	μS
Start-up time		t_{osc}	–	1	5	s
Frequency stability	$\Delta V_{DD} = 100$ mV	Δf/f	–	$0{,}05 \times 10^{-6}$	$0{,}3 \times 10^{-6}$	
Frequency tolerance	device-to-device	Δf/f	–	$\pm 3 \times 10^{-6}$	$\pm 10 \times 10^{-6}$	
Input capacitance		C_i	–	4	–	pF
Output capacitance	$V_{i(p-p)} \leq 50$ mV	C_o	19	24	29	pF
End-of-life detection						
Threshold voltage						
PCA1260	normal and test mode	V_{EOL}	1,20	1,30	1,44	V
PCA1261	test mode only	V_{EOL}	1,20	1,30	1,49	V
Hysteresis of threshold		ΔV_{EOL}	–	10	–	mV
Temperature coefficient		$\frac{\Delta V_{EOL}}{dT}$	–	+ 1,0	–	mV/K
Reset						
Output frequency		f_o	–	32	–	Hz
Output voltage swing	R = 1 MΩ, C = 10 pF	ΔV_o	1,4	–	–	V
Edge time	R = 1 MΩ, C = 10 pF	t_e	–	1	–	μs
Peak input current	note 1	I_{im}	–	320	–	nA
Average input current		$I_{i(av)}$	–	10	–	nA

Note

1. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

TIMING PARAMETERS

section	remark	symbol	value	option	unit
Motor pulse Figs 3 and 4	cycle for motor pulse	t_T	1		s
	motor pulse width	t_B	7,81		ms
	duty factor	t_{DF}	977		μs
	duty factor on	t_{ON}	611		μs
	duty factor off	t_{OFF}	366		μs
	first duty factor on	t_{ONF}	488		μs
	last duty factor on	t_{ONL}	122		μs
Detection Fig. 7	detection sequence	t_D	23,64		ms
	dissipation of energy	t_{DI}	977	1954	μs
	measured cycle	t_{MC}	488		μs
	phase 1	t_{M1}	244		μs
	phase 2 (measure window)	t_{M2}	61		μs
	phase 3	t_{M3}	122		μs
	phase 4	t_{M4}	61		μs
	positive current:				
	PCA1260	P	3	1 to 7	
	PCA1261	P	1		
	negative current:				
	PCA1260	N	5	1 to 7	
	PCA1261	N	2		
Correction sequence Fig. 8	correction sequence	t_C	39,06		ms
	small pulse width	t_{C1}	977		μs
	large pulse width	t_{C2}	7,81		ms
End-of-life Fig. 9	EOL sequence	t_E	4		s
	detection of EOL	t_{E1}	4		s
	motor pulse width	t_{E2}	7,81		ms
	time between pulses	t_{E3}	31,25		ms
Testing Fig. 10	cycles for motor				
	pulses in: Test 1	t_{T1}	62,5		ms
	Test 2	t_{T2}	31,25		ms
	Test 3	t_{T3}	125		ms
	debounce time for RESET = V_{DD}	t_{DEB}	15,7 to 78,1		ms

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

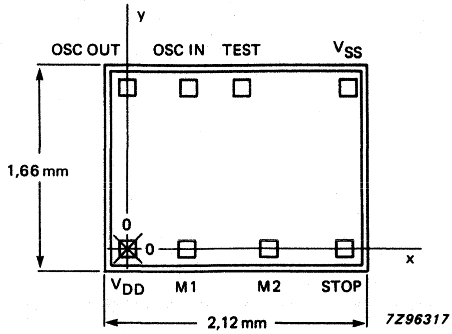


Fig. 11 Bonding pad locations.

Bonding pad dimensions 110 μm x 110 μm
Chip area = 3,41 mm^2

DEVELOPMENT DATA

Table 1 Bonding pad location (dimensions in μm)
All x, y co-ordinates are referenced to the bottom left pad (V_{DD}), see Fig. 11.

pad	x	y
V_{SS}	1795	1290
TEST	925	1290
OSC IN	500	1290
OSC OUT	0	1290
V_{DD}	0	0
M2	485	0
M1	1145	0
STOP	1765	0
chip corner max. value	−160	−160

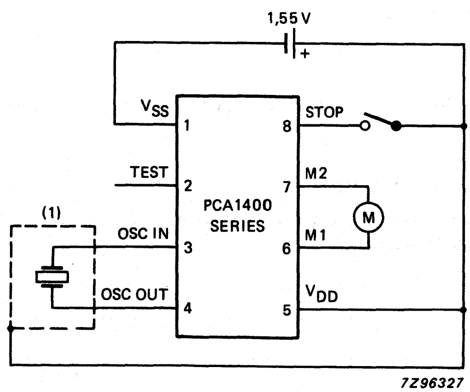
32 kHz WATCH CIRCUIT WITH EEPROM FOR TIMEKEEPING ADJUSTMENT

GENERAL DESCRIPTION

The PCA1400 is a CMOS integrated circuit specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with bipolar stepping motors.

Features

- 32 kHz oscillator, with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Timekeeping adjustment electrically programmable and reprogrammable
- Programming uses only the supply connections
- Motor signal adjustable with the metal mask to customers specifications
- Stop function for time setting
- Fast mode for testing the mechanical part of the watch
- Protection against electrostatic charges
- Immunity against parasitic impedance: 20 MΩ, any pin with respect V_{DD} or V_{SS}
- Low current consumption: typically 200 nA
- Low minimum supply voltage: 1,2 V
- For available types see Table 2



(1) Quartz crystal case to be connected to V_{DD}.

Fig. 1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA14XXT: 8-lead micro-flat-pack; plastic (SOT-144).
PCA14XXU: chip in tray.

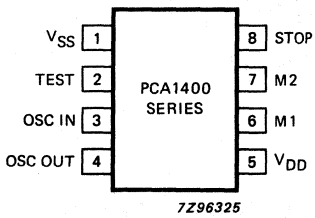


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	supply voltage
6	M1	motor 1 output
7	M2	motor 2 output
8	STOP	motor stop

FUNCTIONAL DESCRIPTION AND TESTING

Normal mode

"STOP" (pin 8), a frequency of 32 Hz is available at the STOP pin.

Stop mode

The motor is stopped by connecting "STOP" (pin 8) to V_{DD}. A motor pulse which has already started cannot be affected by a signal on the STOP input. The first motor pulse will appear one cycle time after disconnecting the stop signal. The STOP input operates after a delay to prevent an accidental motor stop caused by shock or contact bounce.

Test mode 1 (motor test)

"TEST" (pin 2) connected to V_{DD}. For all types the motor output period is 31,25 ms and a pulse width of t_p, the same as in the normal mode.

Test mode 2 (IC test)

"TEST" (pin 2) and "STOP" (pin 8) connected to V_{DD}. For all types the motor output period is 469 ms.

Test mode 3 (timekeeping adjustment, V_{DD} = 5 V)

The adjustment is made approximately every 30 ms instead of every 60 s (2000 time faster). The motor period is increased by 244 μs per bit.

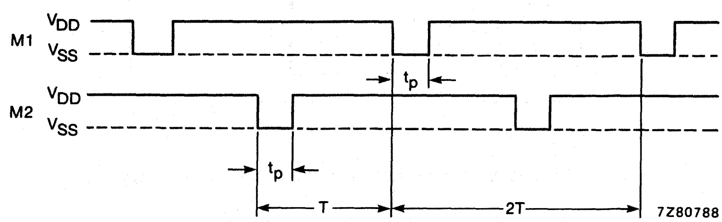


Fig. 3 Motor output waveforms.

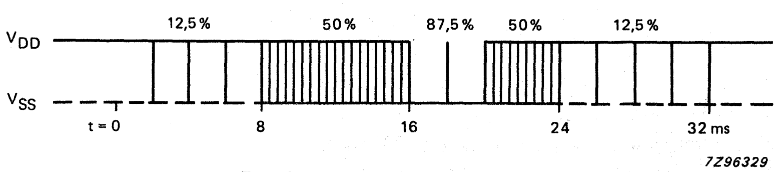


Fig. 4 Motor pulse option.

Timekeeping adjustment

To compensate for the tolerance in the quartz crystal frequency, a number (n) of 4096 Hz are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, which is achieved by the following steps (see Fig. 6):

1. The quartz frequency deviation ($\Delta f/f$) and n are found (see Table 1).
2. V_{DD} is increased to 5,65 V (test mode 3).
3. V_{DD} is pulsed n times between 5,65 V and 4,35 V. The last pulse only goes to 5 V.
4. Wait 150 ms for automatic programming.
5. Check programming from the motor period T (test mode 3).
6. Return to operating mode (step 3 can be omitted for checking only).

Note

Programming can be performed ten times.
Usually the PCA1400 series are delivered with n set to 31.

Table 1 Quartz crystal frequency deviation and n

$\frac{\Delta f}{f} \times 10^{-6}$	n	t (ms) step 5
+ 4,06	1	31,494
+ 8,12	2	31,738
.	.	.
.	.	.
.	.	.
+ 125,86	31	38,814

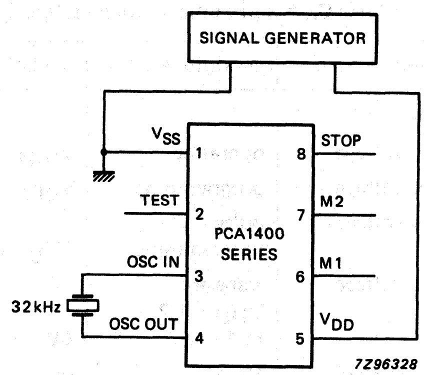


Fig. 5 Programming circuit diagram.

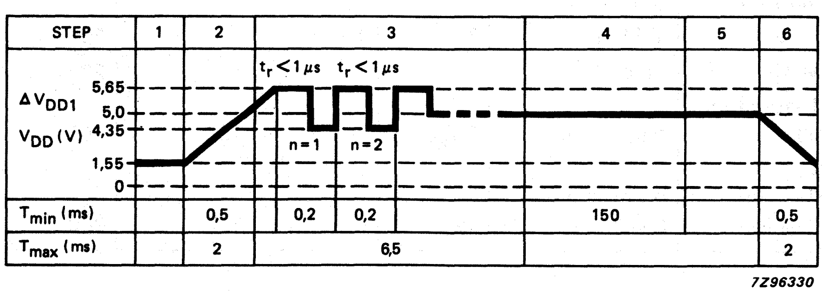


Fig. 6 V_{DD} for programming.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1,8 to + 6	V
All input voltages; note 2	V_I	V_{SS} to V_{DD}	V
Output short-circuit duration		indefinite	
Operating ambient temperature range (with data retention)	T_{amb}	−10 to + 60	°C
Storage temperature range	T_{stg}	−10 to + 100	°C
Resistance against electrostatic discharges		note 3	

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').
3. Three discharges of a 100 pF capacitor at 800 V, through a resistor of 1,5 kΩ (with positive and negative polarity).

CHARACTERISTICS

V_{DD} = 1,55 V; V_{SS} = 0 V; f_{osc} = 32,768 kHz; T_{amb} = 25 °C; crystal: R_s = 15 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_o = 3 pF; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD1}	1,2	1,55	1,8	V
Supply voltage	programming	V_{DD2}	4,9	5,0	5,1	V
Supply voltage	pulse programming	ΔV_{DD1}	0,45	0,50	0,55	V
Supply voltage	transient V_{DD} = 1,2 to 1,8 V	ΔV_{DD}	–	–	0,45	V
Supply current	$R_M = \infty$	I_{DD}	–	200	300	nA
Motor outputs	(see Fig. 3)					
Cycle time	Table 1	T	1	–	60	s
Pulse width	Table 1	t_p	1	–	28	ms
Sum of saturation voltages	R_M = 2 kΩ	ΣV_{sat}	–	120	150	mV
Output short-circuit impedance	between motor pulses	R_{os}	–	150	200	Ω

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Starting voltage		$V_{OSC\ ST}$	–	1,1	1,2	V
Transconductance	$V_{i(p-p)} < 50$ mV	gm	6	15	–	µS
Start-up time		t_{OSC}	–	1	5	s
Frequency stability	$\Delta V_{DD} = 100$ mV	Δf/f	–	$0,1 \times 10^{-6}$	$0,3 \times 10^{-6}$	
Frequency tolerance	quartz tolerance	Δf/f	$+4 \times 10^{-6}$	$+60 \times 10^{-6}$	$+126 \times 10^{-6}$	
Input capacitance	note 1	C_i	–	9	–	pF
Output capacitance	note 1	C_o	–	15	–	pF
Motor stop						
Output frequency		f_o	–	32	–	Hz
Output voltage swing	R = 1 MΩ C = 10 pF	ΔV_o	1,4	–	–	V
Edge time	R = 1 MΩ C = 10 pF	t_e	–	1	–	µs
Peak input current	note 2	I_{im}	–	0,5	–	µA
Average input current	note 2	$I_{i(av)}$	–	30	–	nA
Stop delay		t_{dSTOP}	30	–	65	ms
Test input						
Input current	TEST = V_{DD}	I_i	–	5	–	µA

Notes to the characteristics

1. For PCA1408 and PCA1411; $C_i = 5$ pF, $C_o = 19$ pF.
2. Duty factor is 1 : 16 and RESET = V_{DD} or V_{SS}.

Table 2 Available types

types	cycle time T (s)	pulse width t_p (ms)
PCA1401	1	7,8
PCA1403	20	7,8
PCA1404	5	7,8
PCA1408	20	5,8**
PCA1409	1	5,8
PCA1411	1	7,8**
PCA1412	1	31,2*
PCA1426	20	5,8
PCA1446	1	3,9
PCA1449	12	5,8

* See Fig. 4.
** Fixed pulse width.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

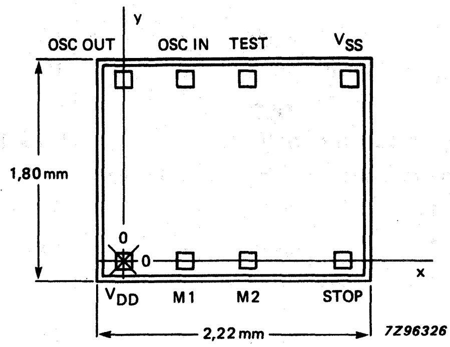


Fig. 7 Bonding pad locations.

Bonding pad dimensions 120 μm x 120 μm
Chip area = 3,9240 mm^2

Table 3 Bonding pad locations (dimensions in μm)
All x, y co-ordinates are referenced to the bottom left pad (V_{DD}), see Fig. 7.

pad	x	y
V_{SS}	1820	1470
TEST	1000	1470
OSC IN	500	1470
OSC OUT	0	1470
V_{DD}	0	0
M1	500	0
M2	1000	0
STOP	1760	0
chip corner max. value	−160	−160

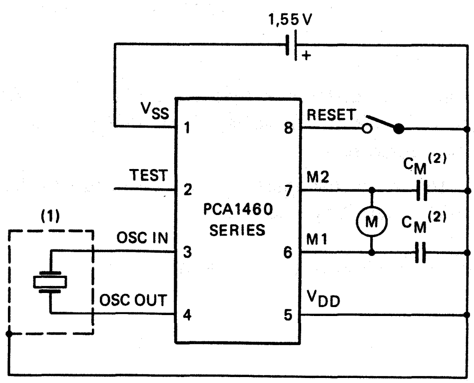
32 kHz WATCH CIRCUIT WITH EEPROM AND ADAPTIVE MOTOR PULSE FOR SILVER OXIDE AND LITHIUM BATTERIES

GENERAL DESCRIPTION

The PCA1460 is a CMOS integrated circuit specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with bipolar stepping motors.

Features

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Timekeeping adjustment electrically programmable and reprogrammable
- A quartz crystal is the only external component required
- Very low current consumption: typically 170 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current, compared with conventional circuits, by self adaption of the motor pulse width according to the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Detector for lithium or silver oxide battery voltage levels
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch as well as the IC itself



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0,5 pF or larger than 20 MΩ.
(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} or V_{SS} should be less than C_M = 80 pF for correct operation of the detection circuit. Driving the motor at its minimum energy, probe and stray capacitance must be avoided.

Fig. 1 Typical application circuit diagram.

PACKAGE OUTLINES

PCA146XT: 8-lead micro-flat-pack; plastic (SOT-144).
PCA146XU: chip in tray.

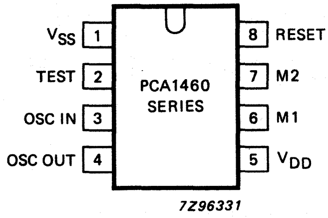


Fig. 2 Pinning diagram.

PINNING

1	V_{SS}	ground (0 V)
2	TEST	test input
3	OSC IN	oscillator input
4	OSC OUT	oscillator output
5	V_{DD}	supply voltage
6	M1	motor 1 output
7	M2	motor 2 output
8	RESET	reset input

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different stages depending on the torque required to turn the motor (Fig. 4). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. When a step is missed a correction sequence will be started (Fig. 3).

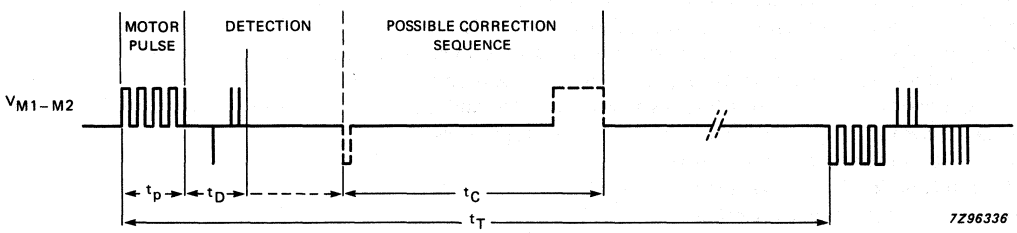


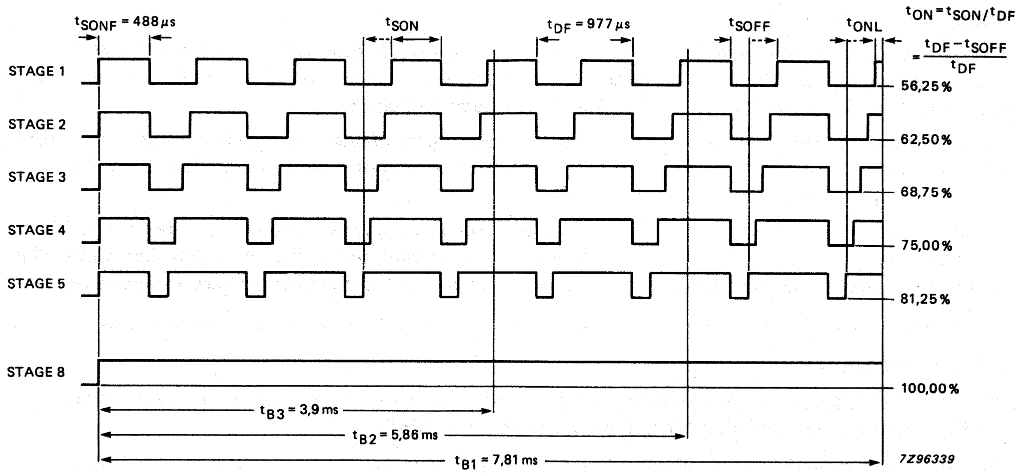
Fig. 3 Possible motor output waveform in normal operation with motor connected.

Motor pulses

The circuit produces motor pulses of six different stages (stage 1 to 5, stage 8). Each stage has two independent modes; silver oxide and lithium. The voltage level of V_{DD} determines which mode is selected (see section ‘Voltage level detector’).

Stages 1 to 5 (both modes) are used in normal operation, stage 8 occurs under the following conditions:

- correction pulse after a missing step (both modes)
- end-of-life mode
- if stage 5 is not enough to turn the motor (both modes)



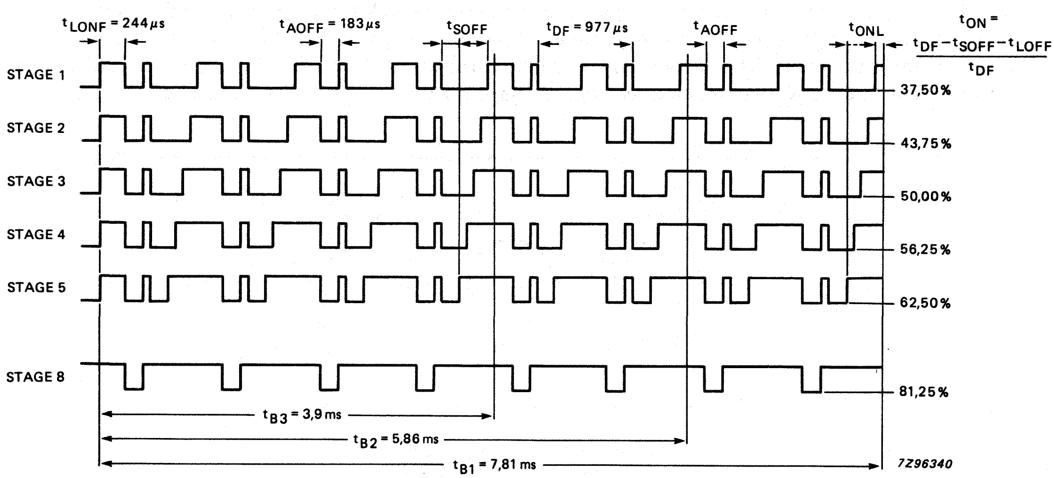
t_{OFF} for stage 1 to 5 = 488 µs − stage x 61 µs

t_{ON} for stage 1 to 5 = 488 µs + stage x 61 µs

Fig. 4 Motor pulses in the silver-oxide mode (V_{DD} = 1,55 V).

DEVELOPMENT DATA

In the silver-oxide mode, the ON state of the motor pulse varies between 56,25% and 100% of the duty factor t_{DF} = 977 µs depending on the stage (Fig. 4). It increases in steps of 6,25% per stage. In the lithium mode, the ON state of the motor pulse is reduced by 18,75% of the duty factor t_{DF} (Fig. 5) to compensate for the increase in the voltage level.



t_{OFF} for stage 1 to 5 = 672 µs − stage x 61 µs

t_{ON} for stage 1 to 5 = 305 µs + stage x 61 µs

Fig. 5 Motor pulses in the lithium mode (V_{DD} = 2,1 V).

Motor pulses (continued)

After a RESET the circuit always starts with stage 1. The circuit continues to operate in stage 1, when all motor pulses have been executed. A failure to execute all motor pulses results in the circuit going into stage 2, this sequence will be repeated through to stage 8.

When the motor pulses at stage 5 are not large enough to turn the motor, stage 8 is implemented for a maximum of 8 minutes with no attempt to keep current consumption low. After stage 8 has been executed the procedure is repeated from RESET.

The circuit operates for 8 minutes at a fixed stage, if every motor pulse is executed. The next 480 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and for a maximum of 8 minutes the motor pulses are increased by one stage.

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{LIT} and V_{EOL} every minute. The first voltage level detection is carried out 30 ms after RESET.

When a lithium voltage level is detected ($V_{DD} \geqslant V_{LIT}$), the circuit starts operating in the lithium mode (Fig. 5).

When the detected V_{DD} voltage level is between V_{LIT} and V_{EOL}, the circuit operates in the silver-oxide mode (Fig. 4).

If the battery end-of-life is detected ($V_{DD} \geqslant V_{EOL}$), the detection and stage control is switched OFF and the waveform produced is an unchopped version of the stage 8 waveform. To indicate this condition the waveform is produced in bursts of 4 pulses every 4 s.

Detection of motor pulses

After a motor pulse, the motor is shorted to V_{DD} for 1 ms. Afterwards the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig. 6 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1. Then the first of 52 possible measurement cycles (t_{MC}) starts to measure the induced current.

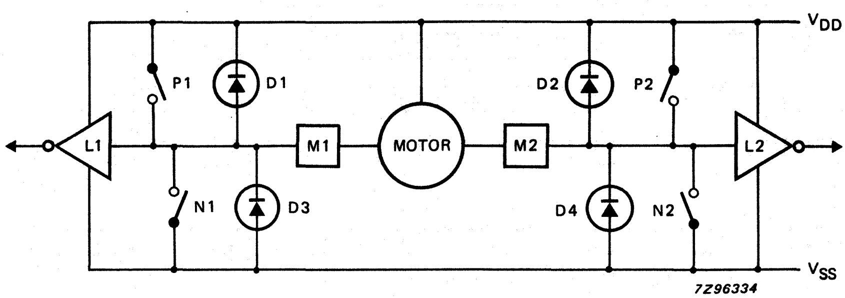


Fig. 6 Motor driving and detecting circuit.

Detection criterion (Figs 7 and 8)

Part 1

- P = 2 number of measured positive current polarities after t_{DI}.

Part 2

- N = 3 number of measured positive current polarities since the first negative current polarity is detected after part 1 (see Fig. 8).

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

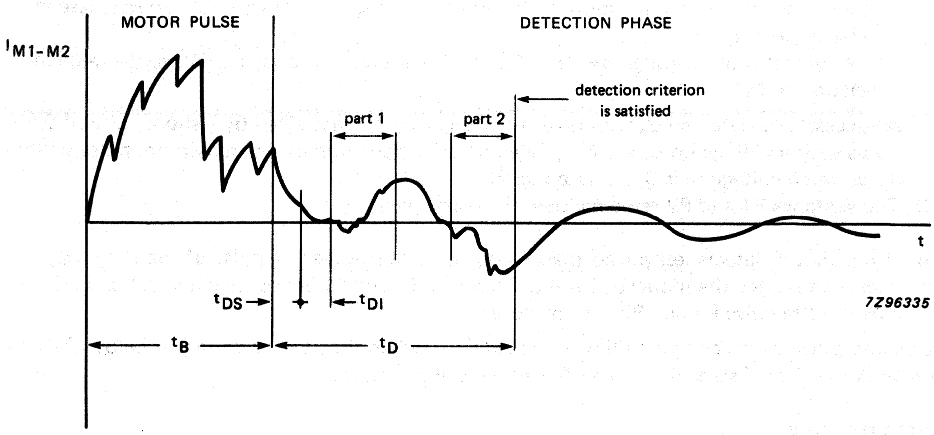


Fig. 7 Typical current waveform of a successfully executed motor pulse.

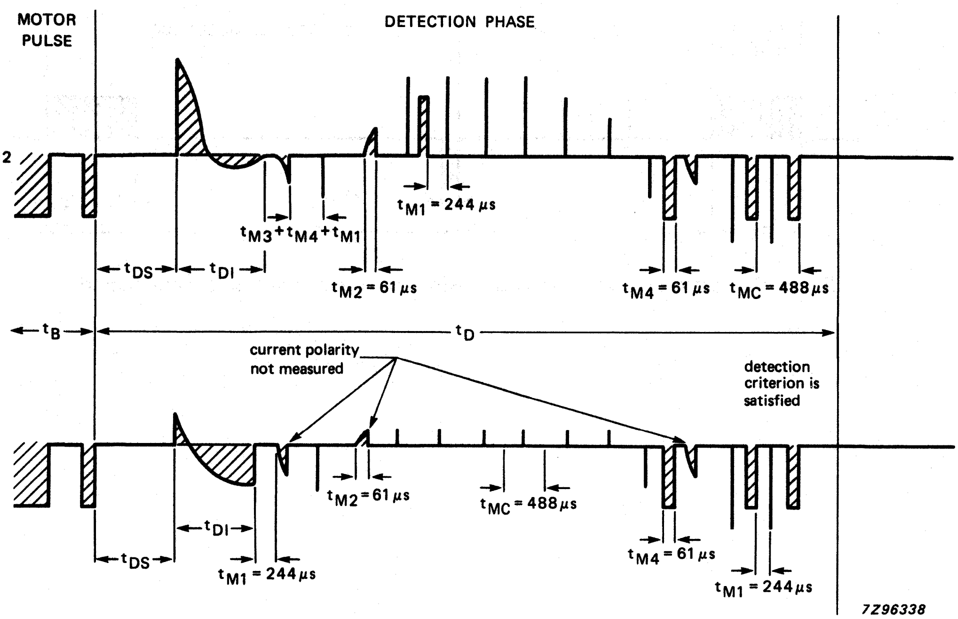


Fig. 8 Detection phase of the current waveform in Fig. 7.

Detection criterion (continued)

Every measurement cycle (t_{MC}) has 4 phases, they are as follows:

Phase 1: (t_{M1}) During t_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.

Phase 2: (t_{M2}) Measures the induced current. During a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is shorted to V_{DD}. Depending on the direction of the interrupted current:

- the current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2;
- the current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1.

A successfully detected current polarity is normally characterized by a short pulse of 0,5 to 10 μs with a voltage up to ± 2,6 V, failed polarity detection by the maximum pulse width of 61 μs and a voltage of ± 0,5 V (see Fig. 9).

Phase 3: (t_{M3}) The switches P1 and P2 remain closed for the time t_{M3}.

Phase 4: (t_{M4}) If the circuit detects less pulses than P and N + 1 respectively, a pulse of the time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed. Otherwise P1 and P2 remain closed.

Detection and pulse width control will be switched OFF, when the battery voltage is below the end-of-life voltage (V_{EOL}) or if stage 5 is not sufficient to turn the motor.

Correction sequence

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 29,30 ms a pulse of stage 8 (t_{C2}) to turn the motor.

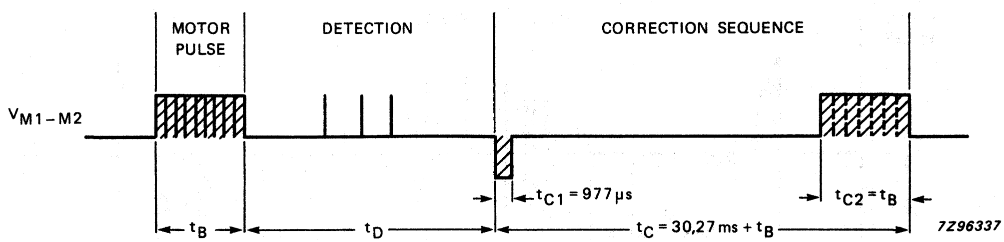


Fig. 9 Correction sequence after a missing motor step with motor connected.

Timekeeping adjustment *

To compensate for the tolerance in the quartz crystal frequency, a number (n) of 8192 Hz are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, which is achieved by the following steps (see Fig. 11):

1. The quartz frequency deviation ($\Delta f/f$) and n are found (see Table 1).
2. V_{DD} is increased to 5,0 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3}.
3. V_{DD} is decreased to 2,5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5,0 V to read the data by pulsing V_{DD} n times to 4,5 V. After the n edge, V_{DD} is decreased to 2,5 V.
7. V_{DD} is increased to 5 V to write the EEPROM and reset the circuit.
8. V_{DD} is decreased to the operating voltage level to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage between two motor pulses to return to operating mode.

Table 1 Quartz crystal frequency deviation and n

$\frac{\Delta f}{f} \times 10^{-6}$	n	t_{T3} (ms) step 2 or 9
+ 2,03	1	31,372
+ 4,06	2	31,494
.	.	.
.	.	.
.	.	.
+ 127,89	63	38,936

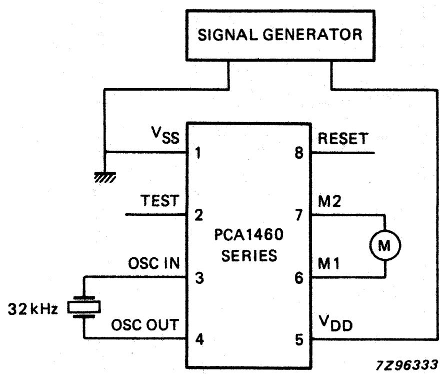
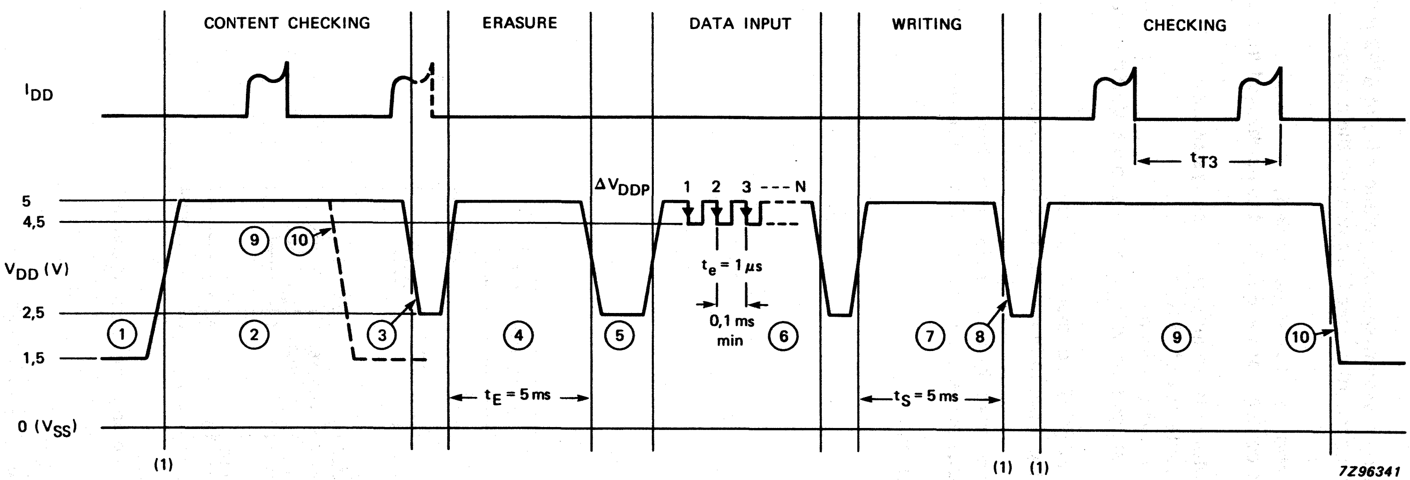


Fig. 10 Programming circuit diagram.

* Programming can be performed ten times.
Usually the PCA1460 series are delivered with n set to 63.



* Rise and fall time should be larger than 1 ms for immediately correct checking.

Fig. 11 V_{DD} for programming.

Power-on reset

For correct operation of the power-on reset the rise time of V_{DD} from 0 V to 2,1 V should be greater than 1 ms. All resetable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geqslant 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of the inhibition, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a 3-state mode and sets the motor pulse width for the next available motor pulse to stage 1 in the silver-oxide mode. A 32 Hz signal without jitter is produced at the TEST pin.

Connecting RESET to V_{SS} activates tests 1 and 2 and disables the inhibition.

In test 1 ($V_{DD} > V_{EOL}$) normal function takes place except the motor pulse period is t_{T1} = 125 ms instead of t_T and the motor pulse level is reduced every second instead of every 8 minutes. In TEST a speeded-up 8 minute signal is available.

If V_{DD} becomes lower than V_{EOL} motor pulses of stage 8 with a time period of t_{T2} = 31,25 ms are produced.

Test and reset mode are terminated by disconnecting the RESET pin. When V_{DD} voltage level is greater than 5 V (test 3), motor pulses of stage 8 with a time period of t_{T3} = 31,25 ms and n x 122 μs are produced to check the contents of the EEPROM. At TEST a speeded-up cycle for motor pulse signal t_T is available. Decreasing V_{DD} voltage level to lower than 2,5 V between two motor pulses returns the circuit to normal operating conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1,8 to + 5	V
All input voltages; note 2	V_I	V_{SS} to V_{DD}	V
Output short-circuit duration		indefinite	
Operating ambient temperature range	T_{amb}	−10 to + 60	°C
Storage temperature range	T_{stg}	−30 to + 100	°C

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisible to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1,55 V; V_{SS} = 0 V; f_{osc} = 32,768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified
Immunity against parasitic impedance = 20 MΩ, from one pin to an adjacent pin.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	T_{amb} = −10 to +60 °C	V_{DD1}	1,2	1,55	2,5	V
Supply voltage	transient within 1,2 V and 2,5 V	ΔV_{DD}	–	–	0,25	V
Supply voltage	programming	V_{DD2}	4,9	5,0	5,1	V
Supply voltage pulse	programming	ΔV_{DDP}	0,45	0,5	0,55	V
Supply current	between motor pulses	I_{DD1}	–	170	260	nA
Supply current	V_{DD} = 2,10 V	I_{DD2}	–	190	300	nA
Supply current	stop mode; pin 8 connected to V_{DD}	I_{DD3}	–	180	280	nA
Supply current	V_{DD} = 2,10 V	I_{DD4}	–	220	360	nA
Supply current	T_{amb} = −10 to +60 °C	I_{DD5}	–	–	600	nA
Motor output						
Saturation voltage Σ (P + N)	R_M = 2 kΩ; T_{amb} = −10 to +60 °C	V_{sat}	–	150	200	mV
Output short-circuit impedance	between motor pulses $I_{transistor}$ < 1 mA	R_{os}	–	200	300	Ω
Oscillator						
Starting voltage		$V_{OSC\ ST}$	1,2	–	–	V
Transconductance	$V_{i(p-p)} \leqslant$ 50 mV	g_m	6	15	–	μS
Start-up time		t_{osc}	–	1	5	s
Frequency stability	ΔV_{DD} = 100 mV	$\Delta f/f$	–	$0,05 \times 10^{-6}$	$0,3 \times 10^{-6}$	
Frequency tolerance	device-to-device	$\Delta f/f$	–	$\pm 3 \times 10^{-6}$	$\pm 10 \times 10^{-6}$	
Input capacitance		C_i	8	10	12	pF
Output capacitance		C_o	12	15	18	pF
Voltage level detector						
Threshold voltage		V_{LIT} V_{EOL}	1,65 1,25	1,80 1,35	1,95 1,45	V V
Hysteresis of threshold		ΔV_{EOL}	–	10	–	mV
Temperature coefficient		$\frac{\Delta V_{EOL}}{dT}$	–	+ 1	–	mV/K

parameter	conditions	symbol	min.	typ.	max.	unit
Reset input						
Output frequency		f_o	–	32	–	Hz
Output voltage swing	R = 1 MΩ; C = 10 pF	ΔV_o	1,4	–	–	V
Edge time	R = 1 MΩ; C = 10 pF	t_e	–	1	–	s
Peak input current	note 1	I_{im}	–	320	–	nA
Average input current		$I_{i(av)}$	–	10	–	nA

Note

1. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

Table 1 Available types

type	pulse width t_B	period	EOL	lithium	detection criterion
PCA1460	t_{B1} = 7,8 ms	t_T = 1 s	yes	yes	P = 2 and N = 3
PCA1461	t_{B1} = 7,81 ms	t_T = 1 s	no	yes	P = 1 and N = 2
PCA1462	t_{B2} = 5,8 ms	t_T = 1 s	yes	yes	P = 2 and P = 3
PCA1463	t_{B3} = 3,9 ms	t_T = 1 s	yes	yes	P = 2 and P = 3

DEVELOPMENT DATA

TIMING PARAMETERS

section	remark	symbol	value	option	unit
Motor pulse Figs 3, 4 and 5	cycle for motor pulse*	t_T	1	5, 10, 12 or 20	ms
	motor pulse width	t_B	7,81	3,9 or 5,9	ms
	duty factor	t_{DF}	977		µs
	last duty factor on	t_{ONL}	61 to 305		µs
Level mode	voltage detection cycle	t_V	60		s
Silver-oxide mode Fig. 4	duty factor on	t_{SON}	550 to 794		µs
	duty factor off	t_{SOFF}	427 to 183		µs
	first duty factor on	t_{SONF}	488		µs
Lithium mode Fig. 5	additional duty factor off	t_{AOFF}	183		µs
	duty factor on	t_{LON}	305 to 611		µs
	duty factor off	t_{LOFF}	672 to 366		µs
	first duty factor on	t_{LONF}	244		µs
End-of-life mode Fig. 11	EOL sequence	t_E	4		s
	motor pulse width	t_{E1}	t_P		ms
	time between pulses	t_{E2}	31,25		ms
Detection Fig. 8	detection sequence	t_D	4,3 to 28,3		ms
	short-circuited motor	t_{DS}	997		µs
	dissipation of energy	t_{DI}	977		µs
	measurement cycle	t_{MC}	488		µs
	phase 1	t_{M1}	244		µs
	phase 2 (measure window)	t_{M2}	61		µs
	phase 3	t_{M3}	122		µs
	phase 4	t_{M4}	61		µs
	positive current polarities	P	2	1 to 6	
	negative current polarities	N	3	1 to 6	
Correction sequence Fig. 9	correction sequence	t_C	t_P + 30,27		ms
	small pulse width	t_{C1}	977		µs
	large pulse width	t_{C2}	t_P		ms
Testing	cycles for motor				
	pulses in: Test 1	t_{T1}	125		ms
	Test 2	t_{T2}	31,25		ms
Fig. 11	Test 3	t_{T3}	31,25 or 39		ms
	debounce time for RESET = V_{DD}	t_{DEB}	13,7 to 78,1		ms

* No option available when EOL indication is required.

4 MHz ALARM CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCA1512 is a CMOS integrated circuit specially suited for battery-operated, quartz-crystal-controlled alarm clocks.

Features

- Oscillator frequency: 4,194 MHz
- Improved low current consumption: typically 25 μA
- Output for bipolar stepping motor with capacitive coupling
  output frequency: 1 Hz
  pulse duration: 1 s
- Alarm output for d.c. buzzer
- Start-stop function
- Test speed-up function

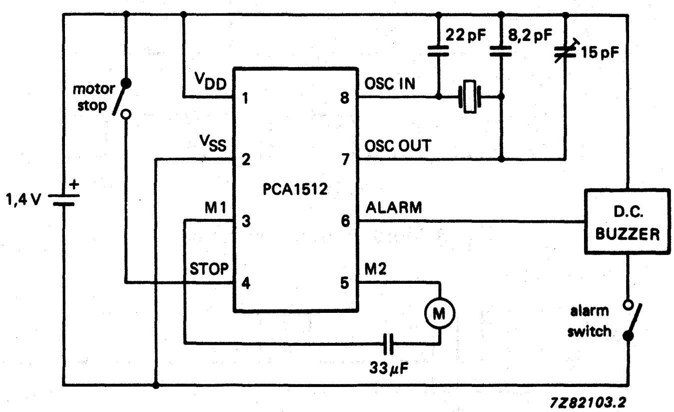


Fig. 1 Typical application circuit diagram.

PACKAGE OUTLINE

PCA1512P: 8-lead DIL; plastic (SOT-97A).

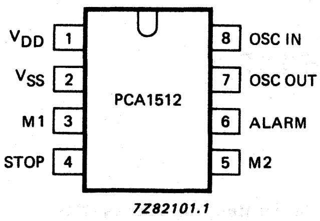


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	supply voltage
2	V_{SS}	ground (0 V)
3	M1	motor 1 output
4	STOP	stop
5	M2	motor 2 output
6	ALARM OUT	alarm output
7	OSC OUT	oscillator output
8	OSC IN	oscillator input

FUNCTIONAL DESCRIPTION AND TESTING

Test speed-up mode

Normal mode: pin 4 open.
Motor stop: pin 4 connected to V_{DD}.
Test mode: feeding a current of 50 μA to 100 μA into pin 4 increases the motor and alarm output frequencies by a factor of 32.
In addition the alarm is modulated with 4069 Hz.

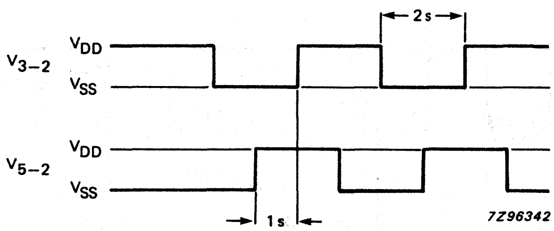


Fig. 3 Motor output waveforms.

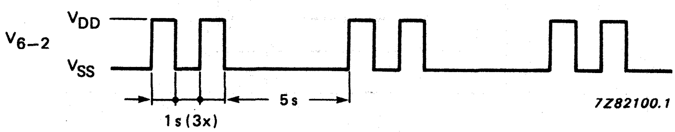


Fig. 4 Alarm output waveform.

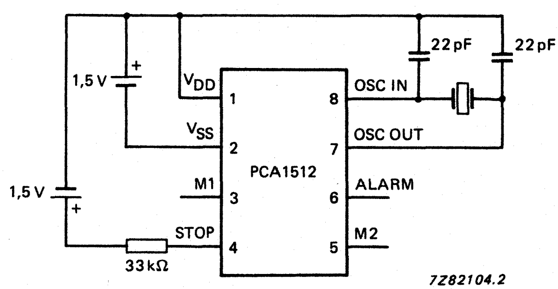


Fig. 5 Test speed-up circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1,7 to + 3 V
Oscillator input voltage; pins 7 and 8; note 2	$V_{7\text{-}2}$; $V_{8\text{-}2}$	0 to V_{DD} V
Input current; pin 4 (test speed-up; Fig. 5)	I_4	max. 1 mA
Output short-circuit duration		indefinite
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−30 to + 125 °C

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 1,4 V; V_{SS} = 0 V; f_{osc} = 4,194 MHz; T_{amb} = 25 °C; crystal: f = 4,194304 MHz; C_L = 12 pF; C_1 = 12 fF; C_o = 3 pF; R_{Smax} = 40 Ω; unless otherwise specified; measured in Fig. 4.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	1,1	–	1,8	V
Supply current	$R_M = \infty$	I_{DD}	–	25	45	μA
Motor output						
Cycle time		T_1	–	2	–	s
Pulse duration		t_{p1}	–	1	–	ms
Current into load	R_M = 200 Ω; V_{DD} = 1,2 V	$I_{3\text{-}5}$	4	–	–	mA
Alarm output						
Output waveform			see Fig. 5			
Sink current	R = 1 kΩ	I_6	2	6	–	μA
Source current	V_{DD} = 1,2 V	I_6	0,3	1	–	mA
Oscillator transconductance	V_{DD} = 1,1 V	g_m	50	–	–	μS
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	$0,2 \times 10^{-6}$	1×10^{-6}	
Stop input current	$V_{4\text{-}2}$ = 1,4 V	I_4	–	4	–	μA
Delay of first output pulse	after release of stop switch	t_d	0,88	–	1	s

4 MHz ALARM CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCA1517 is a CMOS integrated circuit specially suited for battery-operated, quartz-crystal-controlled alarm clocks.

Features

- Oscillator frequency: 4,194 MHz
- Improved low current consumption, typically 25 μA
- Output for bipolar stepping motor
  output frequency: 1 Hz
  pulse duration: 46,8 ms
- Output short-circuited to positive supply between the driving pulses, for damping of the stepper motor
- Alarm output for external n-p-n transistor
- Test speed-up function

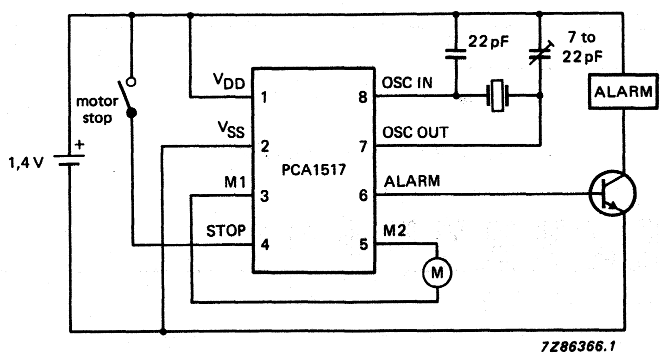


Fig. 1 Typical application circuit diagram.

PACKAGE OUTLINE

PCA1517P: 8-lead DIL; plastic (SOT-97A).

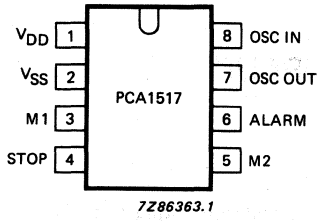


Fig. 2 Pinning diagram.

PINNING

1	V_{DD}	supply voltage
2	V_{SS}	ground (0 V)
3	M1	motor 1 output
4	M STOP	motor stop
5	M2	motor 2 output
6	ALARM OUT	alarm output
7	OSC OUT	oscillator output
8	OSC IN	oscillator input

FUNCTIONAL DESCRIPTION AND TESTING

Test speed-up mode

Normal mode: pin 4 open.
Motor stop: pin 4 connected to V_{DD}.
Test mode: feeding a current of 50 μA into pin 4 increases the motor and alarm output frequencies by a factor of 32.

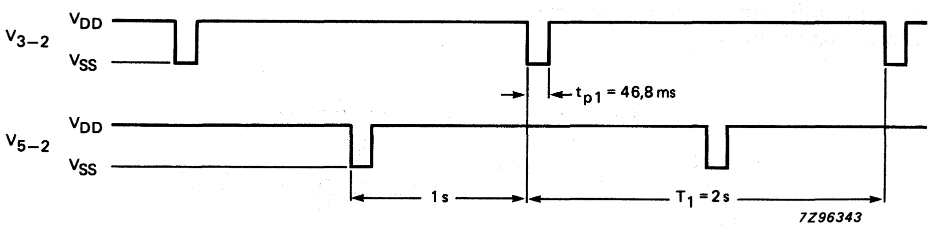


Fig. 3 Motor output waveforms.

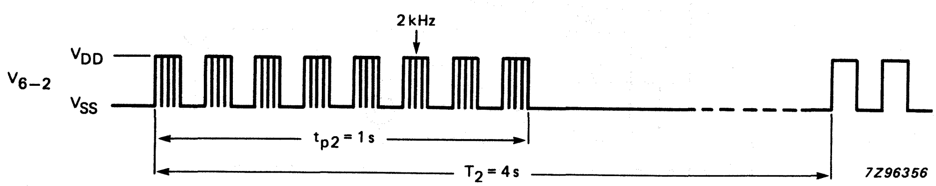


Fig. 4 Alarm output waveform.

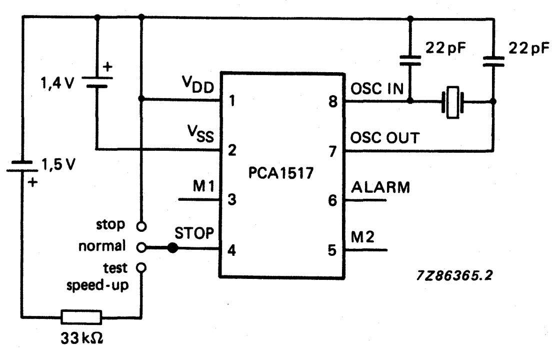


Fig. 5 Test speed-up circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{SS} = 0 V); note 1	V_{DD}	−1,7 to + 3 V
Oscillator input voltage; pins 7 and 8; note 2	$V_{7\text{-}2}$; $V_{8\text{-}2}$	0 to V_{DD} V
Input current; pin 4 (test speed-up; Fig. 5)	I_4	max. 1 mA
Output short-circuit duration		indefinite
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−30 to + 125 °C

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 1,4 V; V_{SS} = 0 V; f_{osc} = 4,194 MHz; T_{amb} = 25 °C; crystal: f = 4,194304 MHz; C_L = 12 pF; C_1 = 1 fF; C_o = 3 pF; R_{Smax} = 40 Ω; unless otherwise specified; measured in Fig. 4.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	1,1	–	1,8	V
Supply current	R_M = ∞	I_{DD}	–	25	45	μA
Motor output						
Cycle time		T_1	–	2	–	s
Pulse duration		t_{p1}	–	46,8	–	ms
Current into load	R_M = 200 Ω; V_{DD} = 1,2 V	$I_{3\text{-}5}$	4	–	–	mA
Alarm output						
Output waveform				see Fig. 5		
Sink current	R = 1 kΩ	I_6	2	6	–	μA
Source current	V_{DD} = 1,2 V	I_6	0,3	1	–	mA
Oscillator transconductance	V_{DD} = 1,1 V	g_m	50	–	–	μS
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	$0,2 \times 10^{-6}$	1×10^{-6}	
Stop input current	$V_{4\text{-}2}$ = 1,4 V	I_4	–	4	–	μA
Delay of first output pulse	after release of stop switch	t_d	0,88	–	1	s

32kHz ALARM CLOCK CIRCUIT WITH EEPROM FOR FREQUENCY ADJUSTMENT

GENERAL DESCRIPTION

The PCA1580 is a silicon-gate CMOS integrated circuit specially suited for battery-operated, quartz-crystal-controlled clocks with bipolar stepper motors.

Features

- Oscillator frequency 32 kHz
- Low current consumption: typically 1,5 μA, maximum 5 μA
- Low minimum supply voltage: 1,1 V
- Alarm input
- Test mode speed-up for fast testing
- Quartz frequency electrically programmable and reprogrammable
- Protected against electrostatic charges

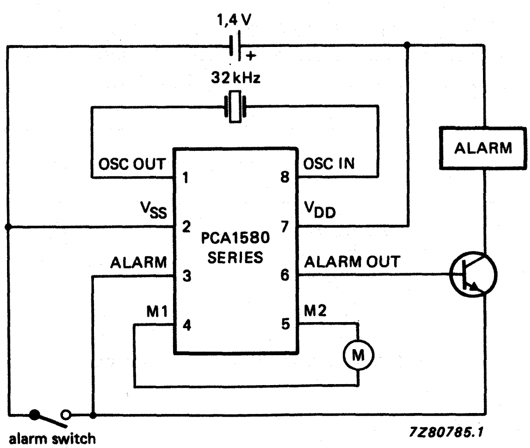


Fig. 1 Typical application circuit diagram.

PACKAGE OUTLINE

PCA158XP: 8-lead DIL; plastic (SOT-97A).
PCA158XT: 8-lead mini-pack; plastic (SO-8; SOT-96C).

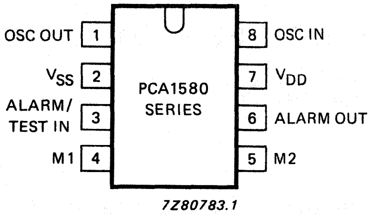


Fig. 2 Pinning diagram.

PINNING

1	OSC OUT	oscillator output
2	V_{SS}	GND, 0 V
3	ALARM/TEST IN	alarm and test input
4	M1	motor 1 output
5	M2	motor 2 output
6	ALARM OUT	alarm output
7	V_{DD}	supply voltage
8	OSC IN	oscillator input

FUNCTIONAL DESCRIPTION AND TESTING

Operating mode

The alarm input is not connected. An output frequency of 256 Hz is provided at pin 3 for test purposes.

Alarm mode

The alarm input is connected to V_{SS}. The alarm signal according to Fig. 4 is provided at pin 6.

Test mode

The alarm input is connected to V_{DD}. The motor output period and pulse width is decreased by a factor of 64. The alarm output periods are also decreased by a factor of 64. In addition the alarm modulation of 2 kHz is suppressed (except in the case of PCA1587).

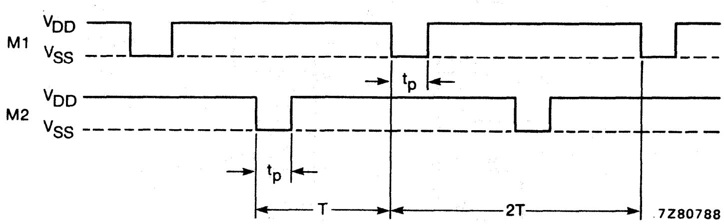


Fig. 3 Motor output waveforms.

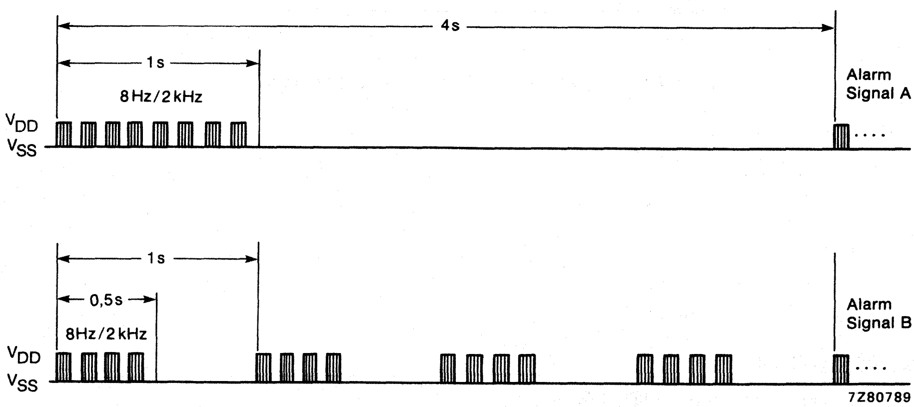


Fig. 4 Alarm output waveforms.

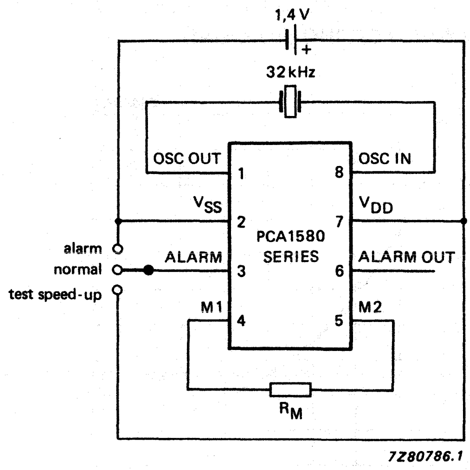


Fig. 5 Test and test speed-up circuit.

Frequency trimming

Frequency trimming is done electrically by programming the oscillator input capacitance to one of 64 values with non-volatile memory. This is done by carrying out the following five steps; Figs 6, 7, 8 and 9 illustrate this procedure.

1. Erasing

With V_{SS} = –1,4 V generator 1 is taken from –1,4 V to 0 V. The device is now in TEST MODE. Erasure is done by increasing V_{SS} to –5,5 V, setting generator 1 to + 1,4 V and supplying a –5,5 V, 1 MHz square-wave signal to pin 6, (output LOW state), from generator 2. Generator 1 is set to 0 V.

2. Checking erasing/zero

With V_{SS} = –1,4 V generator 1 is taken from –1,4 V to 0 V. The device is in TEST MODE and the minimum capacitance is obtained.

3. Measure/data input

The quartz oscillator frequency is now measured. This can be done by the motor output period which is nominally 31,25 ms in this mode. The capacitance is increased by one unit every 1,4 V pulse given by generator 1, and the frequency can be remeasured. This is repeated until the frequency is sufficiently accurate. If the adjustment is too large, it can be restarted with step 2.

4. Writing

The capacitance is fixed by increasing V_{SS} to –5,5 V and supplying a –5,5 V, 1 MHz square-wave signal to pin 6 (output LOW state) from generator 2.

5. Checking writing

With V_{SS} = –1,4 V generator 1 is taken from –1,4 V to 0 V. The device is in TEST MODE and the trimmed capacitance is obtained. The frequency can be checked.

Note

Programming can be performed 10 times. The PCA1580s are normally delivered with the input capacity C_i set to maximum.

FUNCTIONAL DESCRIPTION AND TESTING (continued)

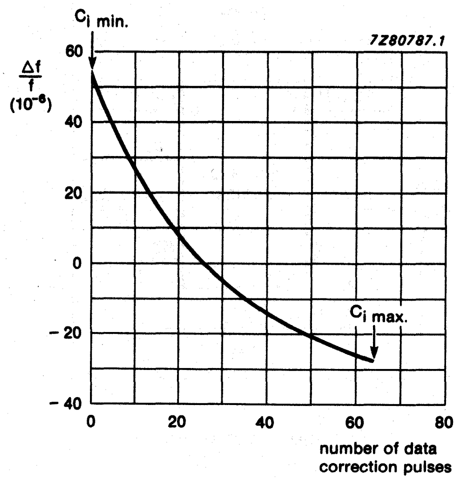


Fig. 6 Typical frequency characteristic. C_1 = 2,8 fF; C_0 = 3 pF; C_L = 10 pF; f = 32,768 kHz.

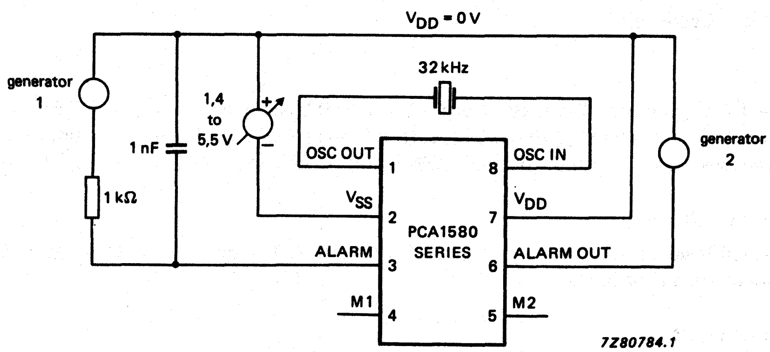


Fig. 7 Frequency trimming circuit.

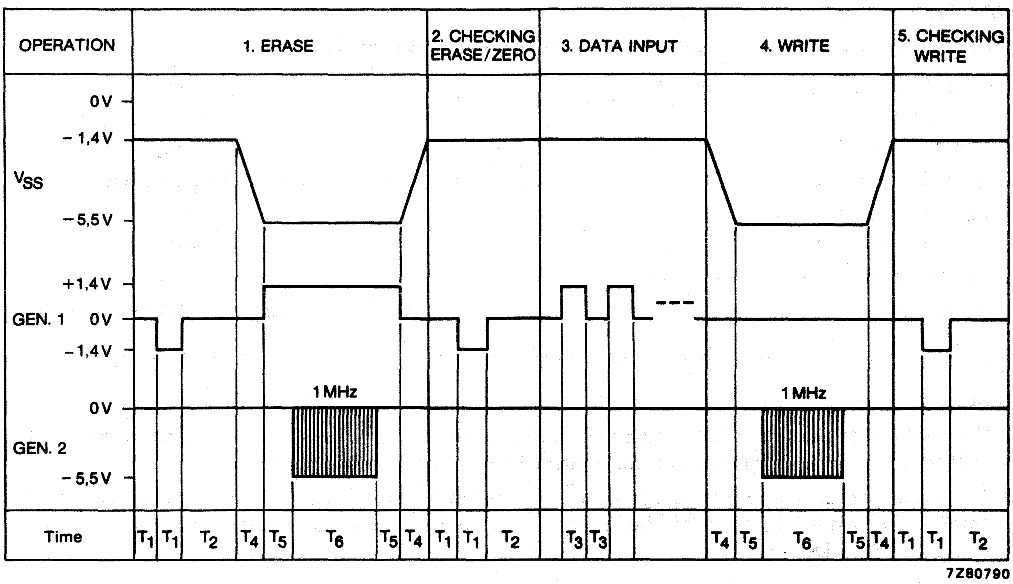


Fig. 8 Frequency trimming signals (V_{DD} = 0 V).

Table 1 Frequency trimming timing requirements.

time	symbol	min.	max.	units
Reset time 1	T_1	1	–	ms
Reset time 2	T_2	5	–	ms
Data pulse width/gap	T_3	100	–	μs
Supply rise/fall time	T_4	1	–	ms
Hold time	T_5	1	–	ms
WRITE/ERASE time	T_6	100	–	ms

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (V_{DD} = 0 V); note 1	V_{SS}	+ 1,8 to −6 V
Input voltage (on all pins except pin 3); note 2	V_I	V_{SS} to V_{DD} V
Input voltage at pin 3	$V_{3\text{-}2}$	V_{SS} to V_{DD} + 1 V
Output short-circuit duration at pins 4, 5 and 6		indefinite
Operating ambient temperature range	T_{amb}	−10 to + 60 °C
Storage temperature range	T_{stg}	−30 to + 125 °C

Notes

1. Connecting the battery at 1,8 V maximum with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Input and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

AVAILABLE TYPES

type number	motor output			alarm signal
	period	pulse width	minimum current	
	T (s)	t_p (ms)	I_L (mA)	
PCA1584	1	46,8	4,0	A
PCA1585	1	46,8	4,0	B
PCA1586	1	15,6	4,3	A
PCA1587	4	15,6	4,3	B*

* Alarm signal not synchronized with alarm on.

CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −1,4 V; f_{osc} = 32,768 kHz; T_{amb} = 25 °C; R_S = 20 kΩ; crystal: C_1 = 2 to 3 fF; C_o = 3 pF; C_L = 10 pF; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{SS1}	−1,1	−	−1,8	V
Supply voltage	starting	V_{SS2}	−1,2	−	−	V
Supply voltage	programming	V_{SS3}	−5,4	−5,5	−5,6	V
Supply current	$R_L = \infty$	I_{DD}	−	1,5	5,0	μA
Motor output						
Period	see available types	T	0,125	−	4	s
Pulse width		t_p	3,9	−	62,5	ms
Current into load	R_M = 200 Ω; V_{SS} = −1,2 V	I_M	see available types			
Output impedance	R_M = 200 Ω	R_o	−	50	−	Ω
Alarm output						
Output waveform	see Figure 4					
Sink current	R = 100 kΩ; V_{SS} = −1,2 V	I_6	1	6	−	μA
Sink current	R = 10 kΩ; V_{SS} = −5,5 V	I_6	−	200	−	μA
Source current	R = 1 kΩ; V_{SS} = −1,2 V	I_6	0,3	1	−	mA
Alarm input						
Delay	note 1		−	−	70	ms
Input current	note 2	I_3	−	2	−	μA
Input current	note 2; V_{SS} = −5,5 V	I_3	−	50	−	μA
Oscillator						
Polarization resistance		R_p	3	10	30	MΩ
Output capacitance	pin 1	C_o	−	24	−	pF
Input capacitance	pin 8					
data pulses	n = 0, note 3	C_i	−	9	−	pF
Input capacitance steps		ΔC	−	0,25	−	pF
Frequency stability	ΔV_{SS} = 100 mV; n = 20	Δf/f	−	$0,4 \times 10^{-6}$	−	
Data retention time	T_{amb} = −10 to + 60 °C	t_{ret}	−	10	−	years

Notes to the characteristics

1. PCA1587 has no defined alarm signal start.
2. These values are averages for the 256 Hz output with 1:1 duty factor.
3. Number of data correction pulses (n).

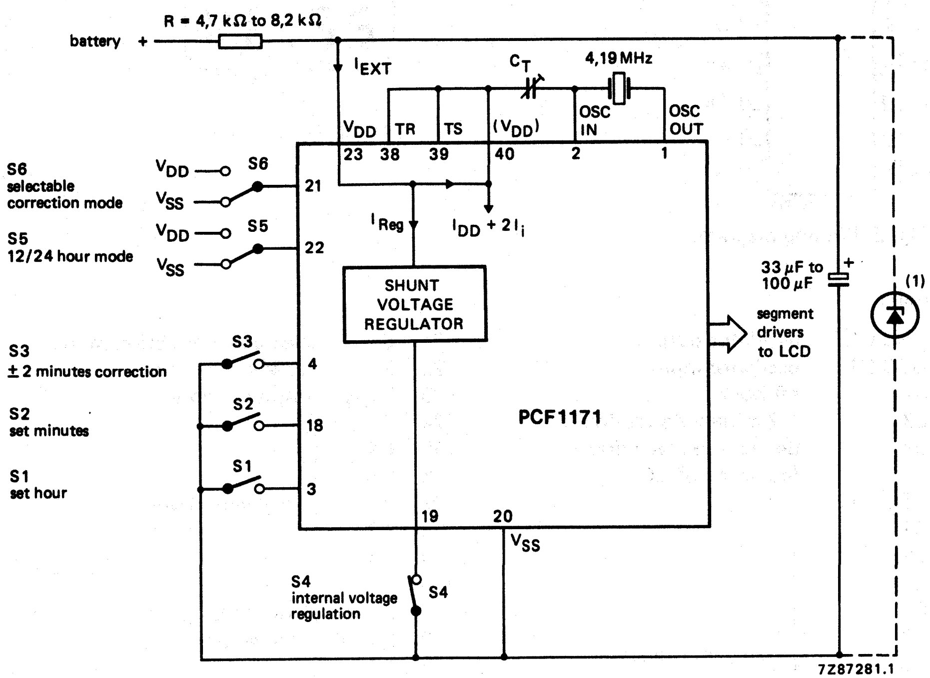
4-DIGIT LCD CAR CLOCK

GENERAL DESCRIPTION

The PCF1171 is a single chip, 4,19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½ or 4-digit liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. A bonding option allows the selection of 12-hour or 24-hour display mode. The circuit is battery operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

Features

- Driving standard 3½ or a 4-digit LCD
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4,19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature range −40 to +85 °C
- 40-lead plastic mini-pack (VSO-40)



(1) Only needed if internal regulation is disconnected.

Fig. 1 Typical application diagram.

Note: From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

PACKAGES OUTLINES

PCF1171BT: 40-lead mini-pack; plastic (VSO-40; SOT-158B).
PCF1171U : uncased chip in tray.

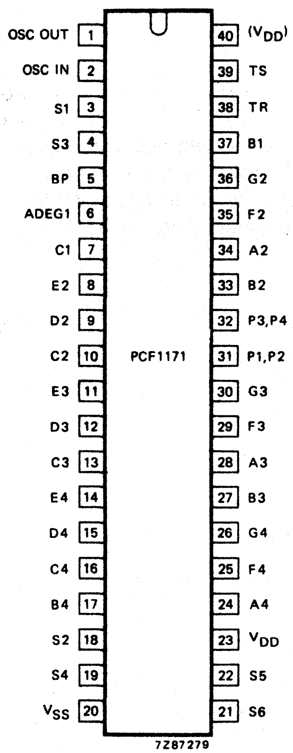


Fig. 2 Pinning diagram.

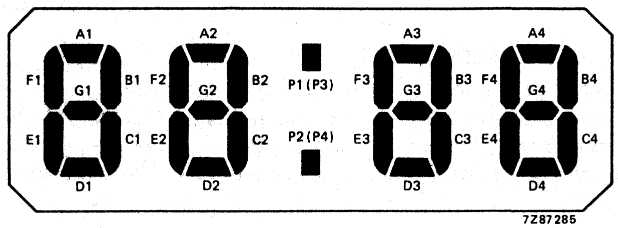


Fig. 3 Segment designation of LCD.

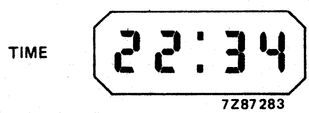


Fig. 4 Display mode.

PINNING

1	OSC OUT	oscillator output
2	OSC IN	oscillator input
3	S1	set hour
4	S3	± 2 minute correction
5	BP	64 Hz backplane driver (common of LCD)
6	ADEG1	segment drivers
7	C1	segment drivers
8	E2	segment drivers
9	D2	segment drivers
10	C2	segment drivers
11	E3	segment drivers
12	D3	segment drivers
13	C3	segment drivers
14	E4	segment drivers
15	D4	segment drivers
16	C4	segment drivers
17	B4	segment drivers
18	S2	set minutes
19	S4	internal voltage regulation
20	V_{SS}	negative supply
21	S6	selectable correction mode
22	S5	12/24-hour mode
23	V_{DD}	positive supply
24	A4	segment drivers
25	F4	segment drivers
26	G4	segment drivers
27	B3	segment drivers
28	A3	segment drivers
29	F3	segment drivers
30	G3	segment drivers
31	P1, P2	colon flashing
32	P3, P4	colon static
33	B2	segment drivers
34	A2	segment drivers
35	F2	segment drivers
36	G2	segment drivers
37	B1	segment drivers
38	TR	test reset; connect to (V_{DD})
39	TS	test speed-up; connect to (V_{DD})
40	(V_{DD})	positive supply for test and oscillator inputs

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

Switch S1

Set hours, S6 selects mode of correction.

Switch S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

Switches S1 and S2

Segment test: If S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00 in the 12-hour mode or 0 : 00 in the 24-hour mode.

Switch options

Switch S3

Time correction ± 2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

Switch S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open; the circuit has to be supplied with an externally regulated voltage.

Switch S5

12-hour display mode: S5 is connected to V_{DD} for 12-hour operation.
24-hour display mode: S5 is connected to V_{SS} for 24-hour operation.

Switch S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65 536. In this mode the maximum input frequency is 100 kHz (external generator at OSC_{IN}). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.

Switch functions also operate in the test mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS} with internal regulation disconnected *	V_{DD}	max.	8 V
Voltage range (any pin)	V_{n-20}	V_{SS} −0,3 to V_{DD} +0,3	V
Storage temperature range	T_{stg}	−55 to +125	°C
Operating ambient temperature range	T_{amb}	−40 to +85	°C

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4,194304 MHz, R_s = 50 Ω, C_L = 12 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (external regulation)	V_{DD}	3	–	6	V
Supply voltage (internal reg. I_{REG} = 1 mA)	V_{DD}	4	5	6	V
Regulation current (with internal regulation)	I_{REG}	0,5	–	5	mA
Current consumption all switches open; without LCD; internal regulation disconnected	I_{DD}	50	250	500	μA
Differential internal impedance at I_{REG} = 1 mA	r_o	–	–	150	Ω
Oscillator (pins 1 and 2)					
start time at $R_{s\,max}$ = 150 Ω	t_{osc}	–	–	200	ms
frequency stability at ΔV_{DD} = 100 mV	$\Delta f/f_{osc}$	–	$0,2 \times 10^{-6}$	1×10^{-6}	
feedback resistance	R_{fb}	0,1	–	1	MΩ
input capacitance	C_i	–	–	9	pF
output capacitance	C_o	19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4) and test inputs, TS, TR (pins 38, 39)					
output current with inputs connected to to V_{SS}	I_i	50	150	500	μA
debounce time	t_d	32	–	150	ms
Segment driver output resistance at ± I_L = 50 μA	R_S	–	1	2,5	kΩ
Backplane driver output resistance at ± I_L = 250 μA	R_{BP}	–	0,2	0,5	kΩ
Backplane driver output frequency	f_{BP}	–	64	–	Hz
LCD d.c. offset voltage at R_L = 200 kΩ; C_L = 1 nF		–	–	±50	mV

Notes to characteristics

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$ (+ LCD current).
2. For correct operation of the oscillator: $V_{DD} \geqslant 3$ V.

* Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

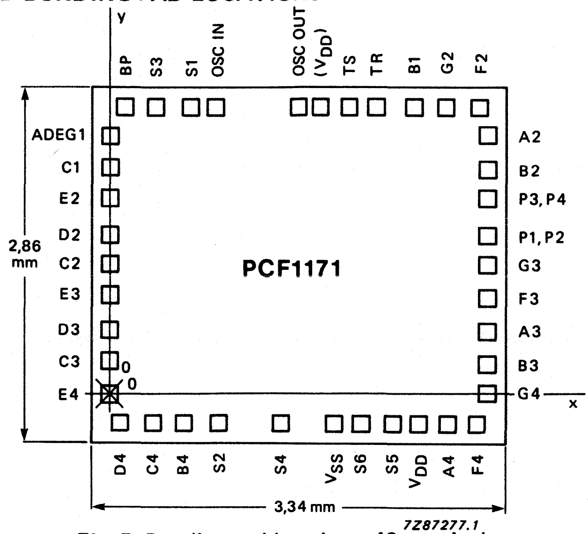


Fig. 5 Bonding pad locations; 40 terminals.

Bonding pad dimensions 100 μm x 100 μm
Chip area = 9,55 mm^2

Table 1 Bonding pad locations (dimensions in μm)
All x/y co-ordinates are referenced to the pad E4, see Fig. 5.

pad	x	y	pad	x	y
OSC OUT	1510	2330	S6	2040	−230
OSC IN	860	2330	S5	2280	−230
S1	640	2330	V_{DD}	2490	−230
S3	370	2330	A4	2710	−230
BP	110	2330	F4	2960	−230
ADEG1	0	2090	G4	3040	10
C1	0	1840	B3	3040	260
E2	0	1570	A3	3040	530
D2	0	1320	F3	3040	780
C2	0	1050	G3	3040	1060
E3	0	800	P1, P2	3040	1310
D3	0	520	P3, P4	3040	1580
C3	0	270	B2	3040	1830
E4	0	0	A2	3040	2100
D4	80	−230	F2	2970	2300
C4	350	−230	G2	2700	2330
B4	600	−230	B1	2450	2330
S2	890	−230	TR	2160	2330
S4	1380	−230	TS	1930	2330
V_{SS}	1820	−230	V_{DD}	1700	2330
Chip corner max. value	−160	−160			

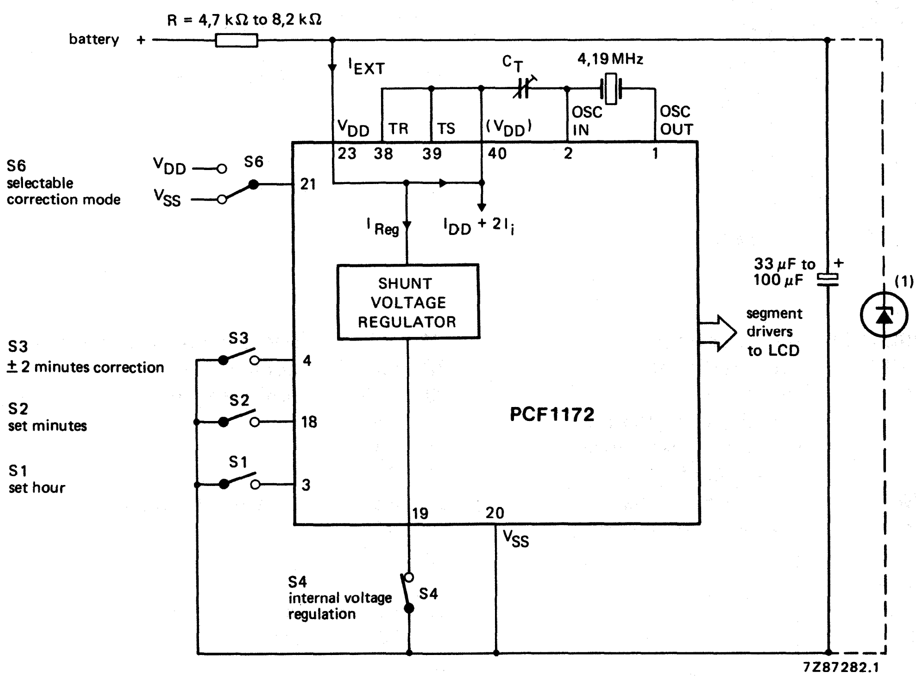
3½-DIGIT LCD CAR CLOCK CIRCUIT

GENERAL DESCRIPTION

The PCF1172 is a single chip, 4,19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½-digit liquid crystal display (LCD) with AM and PM indicators. Two single-pole, single-throw switches accomplish all time setting functions. The circuit is battery operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

Features

- Driving standard 3½-digit LCD with AM and PM indicators
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4,19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature range −40 to +85 °C
- 40-lead plastic-mini pack (VSO-40)



(1) Only needed if internal regulation is disconnected.

Fig. 1 Typical application diagram.

Note: from pin 2 (OSC IN) to any other pin, the stray capacitance should not exceed 2 pF.

PACKAGE OUTLINES

PCF1172BT: 40-lead mini-pack; plastic (VSO-40; SOT-158B).
PCF1172U : uncased chip in tray.

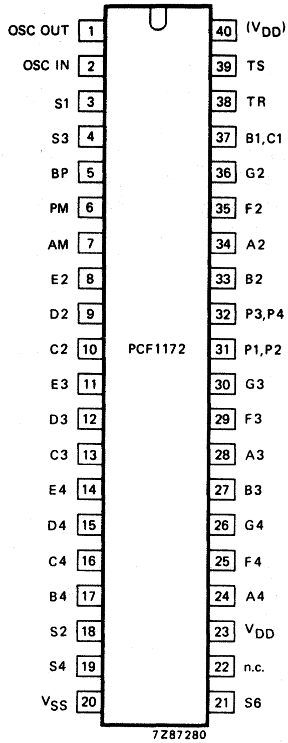


Fig. 2 Pinning diagram.

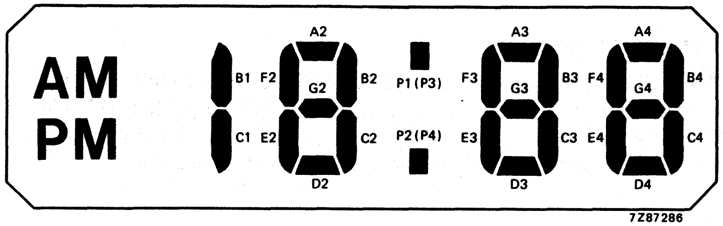


Fig. 3 Segment designation of LCD.

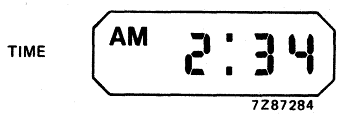


Fig. 4 12-hour display mode.

PINNING

1	OSC OUT	oscillator output
2	OSC IN	oscillator input
3	S1	set hour
4	S3	± 2 minute correction
5	BP	64 Hz backplane driver (common of LCD)
6	PM	segment outputs for PM/AM annunciators
7	AM	
8	E2	segment drivers
9	D2	
10	C2	
11	E3	
12	D3	
13	C3	
14	E4	
15	D4	
16	C4	
17	B4	
18	S2	set minutes
19	S4	internal voltage regulation
20	V_{SS}	negative supply
21	S6	selectable correction mode
22	n.c.	not connected
23	V_{DD}	positive supply
24	A4	segment drivers
25	F4	
26	G4	
27	B3	
28	A3	
29	F3	
30	G3	
31	P1, P2	colon flashing
32	P3, P4	colon static
33	B2	segment drivers
34	A2	
35	F2	
36	G2	
37	B1, C1	
38	TR	test reset; connect to (V_{DD})
39	TS	test speed-up; connect to (V_{DD})
40	(V_{DD})	positive supply for test and oscillator inputs

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

Switch S1

Set hours, S6 selects mode of correction.

Switch S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

Switches S1 and S2

Segment test: If S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00.

Switch options

Switch S3

Time correction ± 2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

Switch S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open; the circuit has to be supplied with an externally regulated voltage.

Switch S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65536. In this mode the maximum input frequency is 100 kHz (external generator at OSC_{IN}). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.
Switch functions also operate in the test mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}			
with internal regulation disconnected*	V_{DD}	max.	8 V
Voltage range (any pin)	V_{n-20}	V_{SS} – 0,3 to V_{DD} + 0,3	V
Storage temperature range	T_{stg}	–55 to +125	°C
Operating ambient temperature range	T_{amb}	–40 to +85	°C

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; crystal: f = 4,194304 MHz, R_s = 50 Ω, C_L = 12 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (external regulation)	V_{DD}	3	–	6	V
Supply voltage (internal regulation I_{REG} = 1 mA)	V_{DD}	4	5	6	V
Regulation current (with internal regulation)	I_{REG}	0,5	–	5	mA
Current consumption all switches open; without LCD; internal regulation disconnected	I_{DD}	50	250	500	μA
Differential internal impedance at I_{REG} = 1 mA	r_o	–	–	150	Ω
Oscillator (pins 1 and 2)					
start time at $R_{s\,max}$ = 150 Ω	t_{osc}	–	–	200	ms
frequency stability at ΔV_{DD} = 100 mV	$\Delta f/f_{osc}$	–	$0,2 \times 10^{-6}$	1×10^{-6}	
feedback resistance	R_{fb}	0,1	–	1	MΩ
input capacitance	C_i	–	–	9	pF
output capacitance	C_o	19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4)					
input current with inputs connected to V_{SS}	I_i	50	150	500	μA
debounce time	t_d	32	–	150	ms
Segment driver output resistance at ± I_L = 50 μA	R_S	–	1	2,5	kΩ
Backplane driver output resistance at ± I_L = 250 μA	R_{BP}	–	0,2	0,5	kΩ
Backplane driver output frequency	f_{BP}	–	64	–	Hz
LCD d.c. offset voltage at R_L = 200 kΩ; C_L = 1 nF		–	–	±50	mV

Notes to characteristics

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$.
2. For correct operation of the oscillator: $V_{DD} \geqslant 3$ V.

* Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

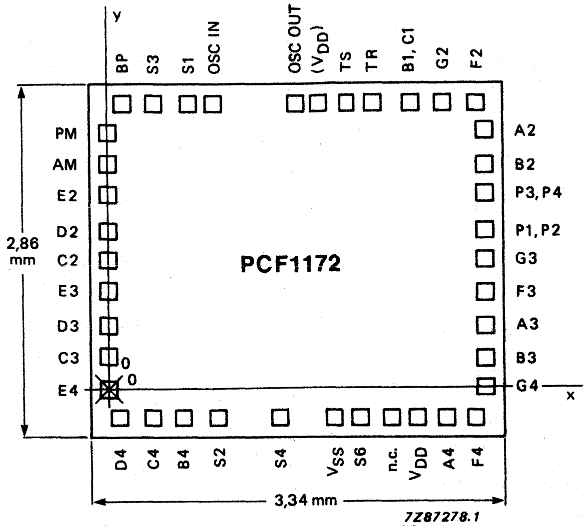
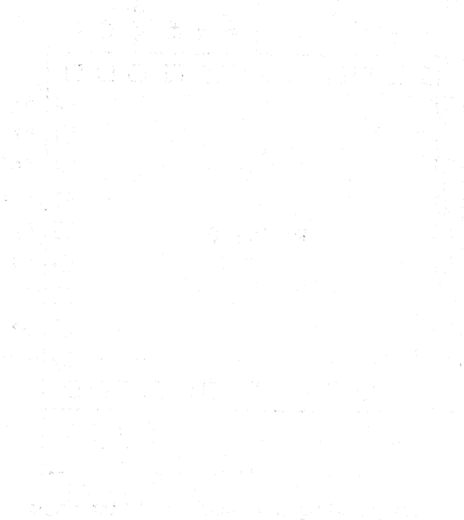


Fig. 5 Bonding pad locations; 40 terminals.

n.c.: not connected
Bonding pad dimensions 100 μm x 100 μm
Chip area = 9,55 mm^2

Table 1 Bonding pad locations (dimensions in μm)
All x/y co-ordinates are referenced to the pad E4, see Fig. 5.

pad	x	y	pad	x	y
OSC OUT	1510	2330	S6	2040	–230
OSC IN	860	2330	n.c.	2280	–230
S1	640	2330	V_{DD}	2490	–230
S3	370	2330	A4	2710	–230
BP	110	2330	F4	2960	–230
PM	0	2090	G4	3040	10
AM	0	1840	B3	3040	260
E2	0	1570	A3	3040	530
D2	0	1320	F3	3040	780
C2	0	1050	G3	3040	1060
E3	0	800	P1, P2	3040	1310
D3	0	520	P3, P4	3040	1580
C3	0	270	B2	3040	1830
E4	0	0	A2	3040	2100
D4	80	–230	F2	2970	2300
C4	350	–230	G2	2700	2330
B4	600	–230	B1, C1	2450	2330
S2	890	–230	TR	2160	2330
S4	1380	–230	TS	1930	2330
V_{SS}	1820	–230	V_{DD}	1700	2330
Chip corner max. value	–160	–160			



4-DIGIT STATIC-LCD CAR CLOCK

GENERAL DESCRIPTION

The PCF1174 is a single chip, 4,19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 4-digit static-liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. The frequency and regulator voltage are electrically programmable via an on-chip EEPROM. The circuit is battery operated via an internal voltage regulator and an external resistor.

Features

- Internal voltage regulator electrically programmable for LCD
- Frequency electrically programmable (no trimming capacitor)
- 4,19 MHz oscillator
- 12 hour or 24 hour mode
- Operating ambient temperature range −40 to + 85 °C
- 40-lead plastic mini-pack (VSO-40)

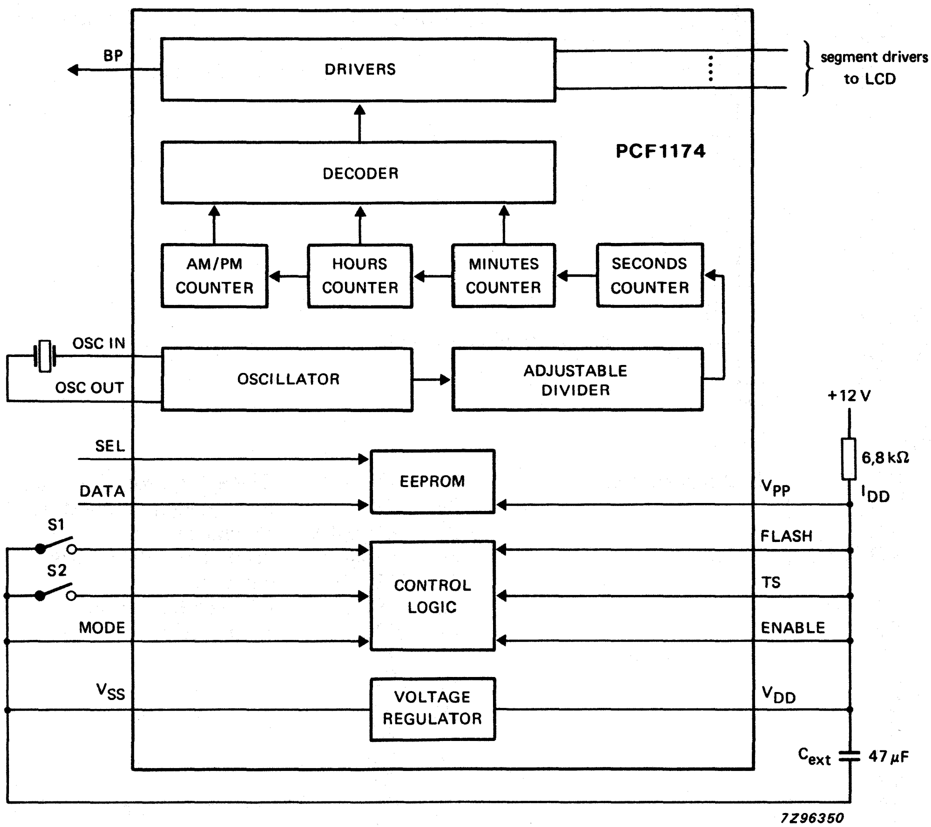


Fig. 1 Typical application diagram.

PACKAGE OUTLINES

PCF1174BT: 40-lead mini-pack; plastic (VSO-40; SOT-158B).
PCF1174U : uncased chip in tray.

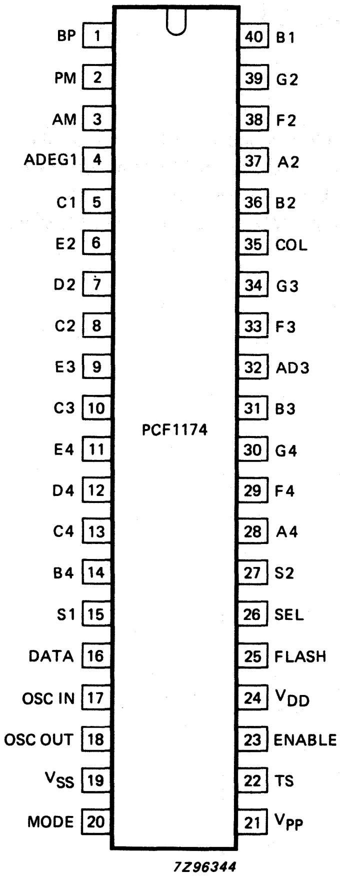


Fig. 2 Pinning diagram.

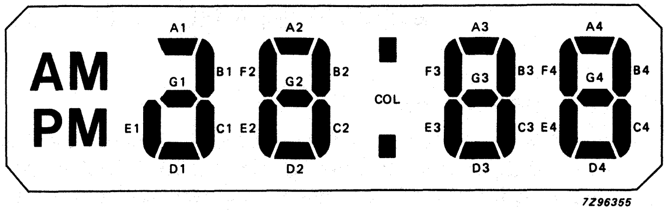
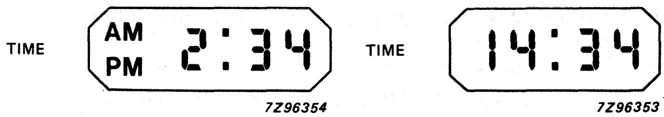


Fig. 3 Segment designation of LCD.



12-hour mode 24-hour mode

Fig. 4 Typical displays.

PINNING

1	BP	backplane output
2	PM	
3	AM	
4	ADEG1	
5	C1	
6	E2	
7	D2	
8	C2	segment drivers
9	E3	
10	C3	
11	E4	
12	D4	
13	C4	
14	B4	
15	S1	set hours
16	DATA	EEPROM, data input
17	OSC IN	oscillator input
18	OSC OUT	oscillator output
19	V_{SS}	negative supply voltage
20	MODE	12/24 hour
21	V_{PP}	EEPROM, programming voltage
22	TS	test speed-up, connect to V_{DD}
23	ENABLE	set enable input
24	V_{DD}	positive supply voltage
25	FLASH	colon option
26	SEL	EEPROM; select input
27	S2	set minutes
28	A4	
29	F4	
30	G4	
31	B3	
32	AD3	
33	F3	
34	G3	segment drivers
35	COL	
36	B2	
37	A2	
38	F2	
39	G2	
40	B1	

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs static data to the LCD. The generation of the backplane signal (BP) and the output signals are shown in Fig. 5. Each segment is driven by an individual output. The circuit is suitable for LCDs with a single backplane.

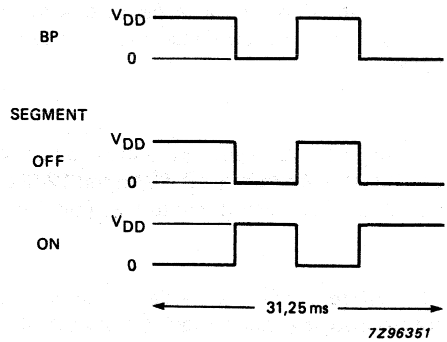


Fig. 5 Backplane and output signals.

The average voltages across the segments are:

$V_{ON(RMS)} = V_{DD}$.
$V_{OFF(RMS)} = 0$ V.

LCD voltage

The adjustable voltage regulator controls V_{DD} (see section 'LCD voltage programming'). The voltage V_{DD} remains almost constant over the ambient temperature range, giving good LCD contrast.

12/24-hour mode

When MODE is connected to V_{DD} the clock is in 12-hour mode.
When MODE is connected to V_{SS} the clock is in 24-hour mode.

Power-on

After connecting the supply, the clock starts from:

1:00 AM; 12-hour mode.
0:00 ; 24-hour mode.

Colon

When FLASH is connected to V_{SS}, COL is a static colon output.
When FLASH is connected to V_{DD}, COL is a flashing colon output (1 Hz).

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate use of single-pole, single-throw contacts. A debounce circuit is integrated as protection against contact debounce and parasitic voltages.

Set enable

When ENABLE is connected to V_{DD}, the inputs S1 and S2 are enabled.
When ENABLE is connected to V_{SS}, the inputs S1 and S2 are disabled.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the minutes displayed advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS} all LCD segments are switched on. When S1 and S2 are disconnected the display is reset, the clock starts at 1:00 AM in the 12-hour mode or 0:00 in the 24-hour mode. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD} the device is in normal mode. By connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing the quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up but for safety it should normally be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up but for reasons of safety it should normally be connected to V_{DD}.

LCD voltage programming

A pulse is applied to V_{PP} (see Fig. 6) to commence programming. When SEL (pin 26) is left open LCD voltage programming is selected. Pulses are applied to the DATA input (pin 16). The first pulse clears the EEPROM, after each subsequent pulse the voltages $V_{DD} - V_{SS}$ are measured until the required voltage level is reached (3 to 6 V) then a store pulse is applied, setting the LCD voltage. To reach 3 to 6 V there is an overlap. Table 1 shows the typical voltage obtained for each applied pulse (n).

Frequency

Electronic adjustment of the frequency eliminates the requirement for an external trimming capacitor. The quartz frequency has been positively offset (nominal deviation + 60×10^{-6}) by capacitors at the oscillator input and output. Depending on the actual deviation a number of (n) 256 kHz pulse are inhibited every second of operation.

Frequency programming

Frequency deviation ($\Delta f/f$) is measured and the required number of pulses (n) found by using Table 2. SEL is connected to V_{SS} allowing programming of the frequency. A pulse is applied to V_{PP} (see Fig. 6) to commence programming. A number (n) of pulses and a store pulse are applied to the DATA input. This is quickly checked by measuring the backplane period in this mode. SEL is then released.

Note: Programming can be performed 10 times. The PCF1174s are normally delivered with the device set at n = 31.

Table 1

number of pulses n	supply voltage V_{DD} (V)
1	2,70
2	2,85
3	3,00
.	.
.	.
.	.
31	7,20

Table 2 (Δt = 3,8 μs)

frequency deviation $\Delta f/f$	number of pulse n	backplane period ms
+ 3,8	1	15,629
+ 7,6	2	15,633
+ 11,4	3	15,636
.	.	.
.	.	.
.	.	.
+ 117,8	31	15,743

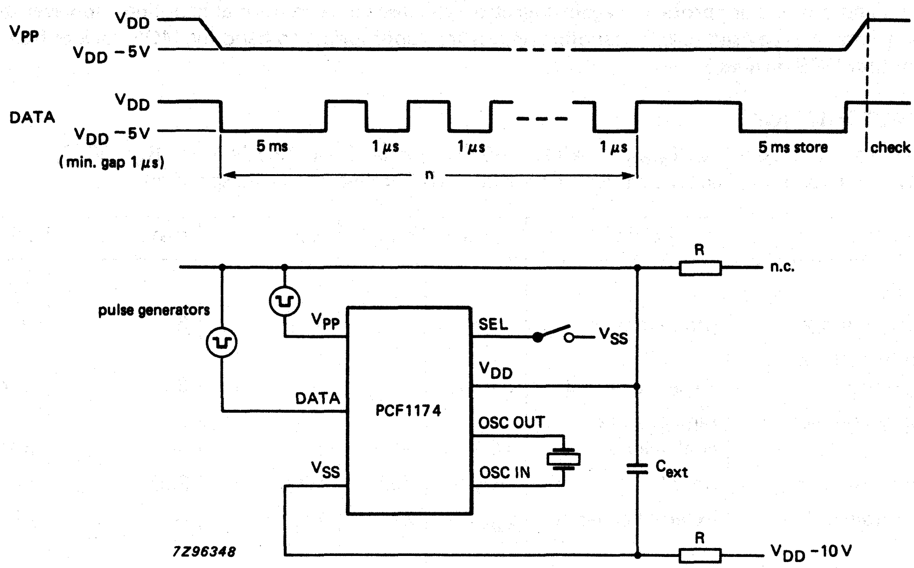


Fig. 6 Programming diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current (V_{SS} = 0 V); note 1	I_{DD}	max.	3 mA
Voltage range (any pin except V_{PP} and DATA); note 2	V_{I1}		–0,3 to V_{DD} + 0,3 V
Voltage range V_{PP} and DATA	V_{I2}		–3,0 to V_{DD} + 0,3 V
Storage temperature range (unprogrammed)	T_{stg}		–55 to + 125 °C
Operating ambient temperature range	T_{amb}		–40 to + 85 °C

Notes

1. Connecting the supply voltage with reverse polarity will not harm the circuit.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C; crystal: f = 4,194304 MHz, R_s = 50 Ω, C_L = 12 pF; maximum frequency tolerance = ± 30 x 10^{-6}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	programmed	V_{DD}	3	–	6	V
Supply voltage variation	S1 or S2 closed	ΔV_{DD}	–	–	50	mV
Supply voltage	temperature coefficient	TC	–	0	–	mV/K
Supply current	note 1	I_{DD}	700	1000	2000	μA
Capacitance	external capacitor	C_{ext}	22	47	–	μF
Oscillator						
Start time	$R_{s\,max}$ = 150 Ω	t_{osc}	–	–	200	ms
Frequency deviation	nominal	Δf/f	0	+ 60 x 10^{-6}	+ 120 x 10^{-6}	
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	–	1 x 10^{-6}	
Input capacitance		C_i	–	11	–	pF
Output capacitance		C_o	–	24	–	pF
Feedback resistance		R_{fb}	300	1000	3000	kΩ
Inputs	S1, S2, TS, SEL, DATA					
Output current	connected to V_{SS}	I_i	25	–	100	μA
Debounce time	S1 and S2 only	t_d	30	65	100	ms

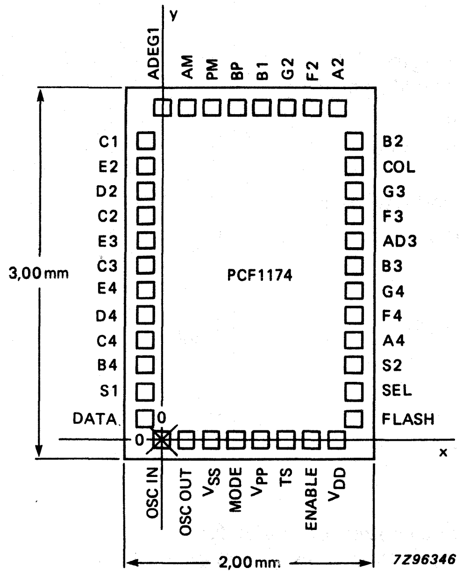
parameter	conditions	symbol	min.	typ.	max.	unit
Input V_{PP}						
Output current	$V_{PP} = V_{DD} - 5$ V OSCIN = V_{SS} or V_{DD}	I_{i2}	125	–	500	μA
Output current	during programming	I_{i2}	–	500	–	μA
Backplane	high and low levels					
Output resistance	± 100 μA	R_{bp}	–	–	1	kΩ
Segment						
Output resistance	± 100 μA	R_{seg}	–	–	3	kΩ
LCD						
D.C. offset voltage	200 kΩ/1 nF	V_{dc}	–	–	50	mV

Notes to the characteristics

1. The external resistor R must be chosen appropriately:
   Example: V_{DD} = 5 V, R max. = (12 V – 5 V)/ 700 μA = 10 kΩ
   V_{DD} = 5 V, R typ. = (12 V – 5 V)/1000 μA = 7 kΩ (more reserve).

DEVELOPMENT DATA

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 6 mm²
Bonding pad dimensions: 100 μm x 100 μm

Fig. 7 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm)
All x/y co-ordinates are referenced to the bottom left pad (OSC_{IN}), see Fig. 7.

pad	x	y	pad	x	y
BP	600	2676	V_{PP}	800	0
PM	400	2676	TS	1000	0
AM	200	2676	ENABLE	1200	0
ADEG1	0	2676	V_{DD}	1400	0
C1	−138	2448	FLASH	1538	168
E2	−138	2228	SEL	1538	388
D2	−138	2008	S2	1538	608
C2	−138	1808	A4	1538	808
E3	−138	1608	F4	1538	1008
C3	−138	1408	G4	1538	1208
E4	−138	1208	B3	1538	1408
D4	−138	1008	AD3	1538	1608
C4	−138	808	F3	1538	1808
B4	−138	608	G3	1538	2008
S1	−138	388	COL	1538	2208
DATA	−138	168	B2	1538	2448
OSC IN	0	0	A2	1400	2676
OSC OUT	200	0	F2	1200	2676
V_{SS}	400	0	G2	1000	2676
MODE	600	0	B1	800	2676
chip corner max. value	−300	−160			

4-DIGIT DUPLEX-LCD CAR CLOCK

GENERAL DESCRIPTION

The PCF1175 is a single chip, 4,19 MHz CMOS clock circuit indicating hours and minutes, It is designed to drive a 4-digit duplex liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. The frequency and regulator voltage are electrically programmable via an on-chip EEPROM. The circuit is battery operated via an internal voltage regulator and an external resistor.

Features

- Internal voltage regulator electrically programmable for LCD
- Frequency electrically programmable (no trimming capacitor)
- LCD voltage adjusts with temperature for good contrast
- 4,19 MHz oscillator
- 12 hour or 24 hour mode
- Operating ambient temperature range –40 to + 85 °C
- 28-lead plastic mini-pack

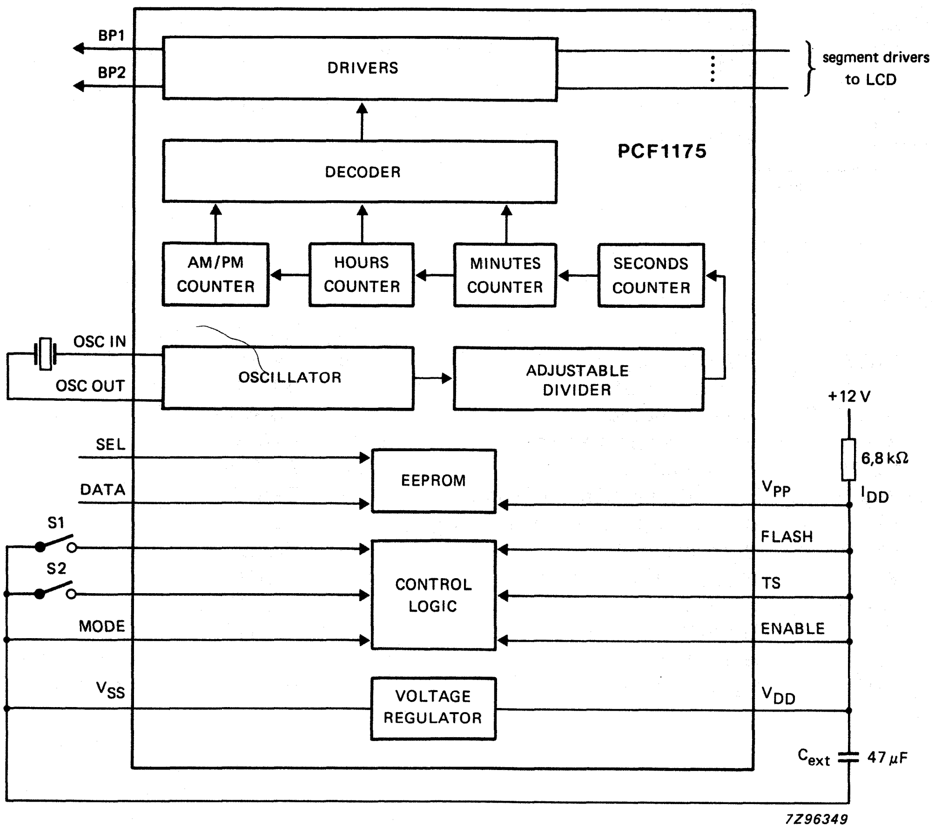


Fig. 1 Typical application diagram.

PACKAGE OUTLINES

PCF1175T: 28-lead mini-pack; plastic (SO-28; SOT-136A).
PCF1175U: uncased chip in tray.

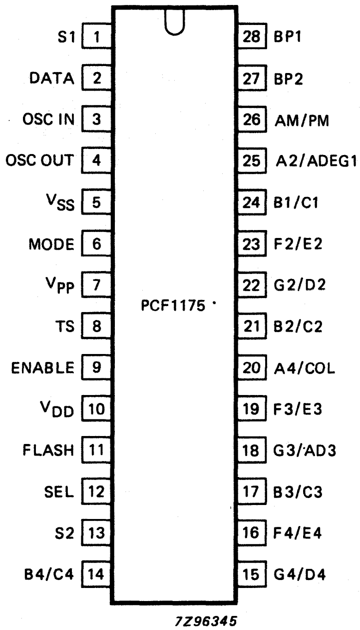


Fig. 2 Pinning diagram.

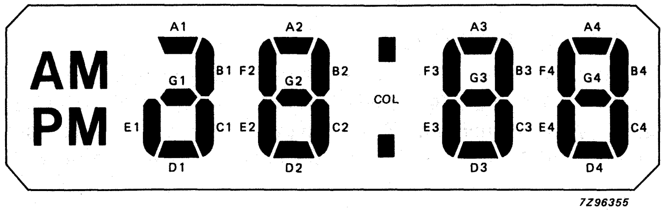
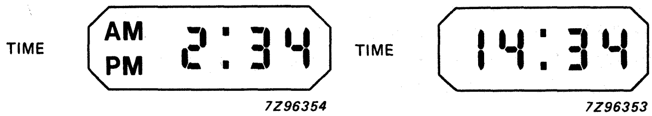


Fig. 3 Segment designation of LCD.



12-hour mode

24-hour mode

Fig. 4 Typical displays.

PINNING

1	S1	set hours	15	G4/D4	segment drivers
2	DATA	EEPROM, data input	16	F4/E4	
3	OSC IN	oscillator input	17	B3/C3	
4	OSC OUT	oscillator output	18	G3/AD3	
5	V_{SS}	negative supply voltage	19	F3/E3	
6	MODE	12/24 hour	20	A4/COL	
7	V_{PP}	EEPROM; programming voltage	21	B2/C2	
8	TS	test speed-up mode; connect to V_{DD}	22	G2/D2	
9	ENABLE	set enable input	23	F2/E2	
10	V_{DD}	positive supply voltage	24	B1/C1	
11	FLASH	colon option	25	A2/ADEG1	
12	SEL	EEPROM, select input	26	AM/PM	
13	S2	set minutes	27	BP2	backplane 2
14	B4/C4	segment drivers	28	BP1	backplane 1

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs multiplexed data 1 : 2 (duplex) to the LCD. The generation of the two backplane signals (BP1 and BP2) with three level waveforms and the output signals are shown in Fig. 5. Each segment driver drives two segments of the LCD (segment 1 uses BP1, segment 2 uses BP2). The LCD must be connected appropriately (see pinning diagram showing segment 1/segment 2).

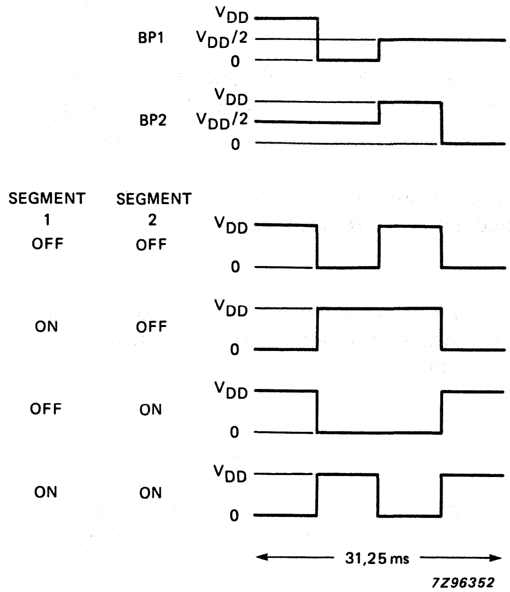


Fig. 5 Backplane and output signals.

The average voltages across the segments are:

$V_{ON(RMS)} = 0{,}79\ V_{DD}$.
$V_{OFF(RMS)} = 0{,}35\ V_{DD}$.

LCD voltage

The adjustable voltage regulator controls V_{DD} (see section 'LCD voltage programming'). When voltage V_{DD} is adjusted to 4,5 V at + 25 °C, the voltage will be between 5 to 6 V at −40 °C and between 3 to 4 V at + 85 °C, giving good contrast.

12/24-hour mode

When MODE is connected to V_{DD} the clock is in 12-hour mode.
When MODE is connected to V_{SS} the clock is in 24-hour mode.
When MODE is left open the clock changes from 12-hour to 24-hour mode or from 24-hour to 12-hour mode after reset.

Power-on

After connecting the supply, the clock start from:

1:00 AM; 12-hour mode if MODE is connected to V_{DD}.
0:00 ; 24-hour mode if MODE is connected to V_{SS}.
0:00 ; 24-hour mode if MODE is left open.

Colon

When FLASH is connected to V_{SS}, COL is a static colon output.
When FLASH is connected to V_{DD}, COL is a flashing colon output (1 Hz).

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate use of single-pole, single-throw contacts. A debounce circuit is integrated as protection against contact debounce and parasitic voltages.

Set enable

When ENABLE is connected to V_{DD}, the inputs S1 and S2 are enabled.
When ENABLE is connected to V_{SS}, the inputs S1 and S2 are disabled.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the minutes displayed advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the second counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS} all LCD segments are switched on. When S1 and S2 are disconnected the display is reset and changes the 12-hour to 24-hour mode or the 24-hour to 12-hour mode when MODE (pin 6) is left open. The clock starts at 1:00 AM in the 12-hour mode or 0:00 in the 24-hour mode. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD} the device is in normal mode. By connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing the quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up but for safety it should normally be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up but for reasons of safety it should normally be connected to V_{DD}.

LCD voltage programming

A pulse is applied to V_{PP} (see Fig. 6) to commence programming. When SEL (pin 12) is left open LCD voltage programming is selected. Pulses are applied to the DATA input (pin 2). The first pulse clears the EEPROM, after each subsequent pulse the voltages $V_{DD} - V_{SS}$ are measured until the required voltage level is reached (4,5 V) then a store pulse is applied, setting to LCD voltage. Table 1 shows the typical voltage obtained for each applied pulse (n).

Frequency

Electronic adjustment of the frequency eliminates the requirement for an external trimming capacitor. The quartz frequency has been positively offset (nominal deviation + 60×10^{-6}) by capacitors at the oscillator input and output. Depending on the actual deviation a number of (n) 256 kHz pulses are inhibited every second of operation.

Frequency programming

Frequency deviation ($\Delta f/f$) is measured and the required number of pulses (n) found by using Table 2. SEL is connected to V_{SS} allowing programming of the frequency. A pulse is applied to V_{PP} (see Fig. 6) to commence programming. A number (n) of pulses and a store pulse are applied to the DATA input. This is quickly checked by measuring the backplane period in this mode. SEL is then released.

Note: Programming can be performed 10 times. The PCF1175s are normally delivered with the device set at n = 31.

Table 1

number of pulses n	supply voltage V_{DD} (V)
1	2,70
2	2,85
3	3,00
.	.
.	.
.	.
31	7,20

Table 2 (Δt = 3,8 μs)

frequency deviation $\Delta f/f$	number of pulse n	backplane period ms
+ 3,8	1	15,629
+ 7,6	2	15,633
+ 11,4	3	15,636
.	.	.
.	.	.
.	.	.
+ 117,8	31	15,743

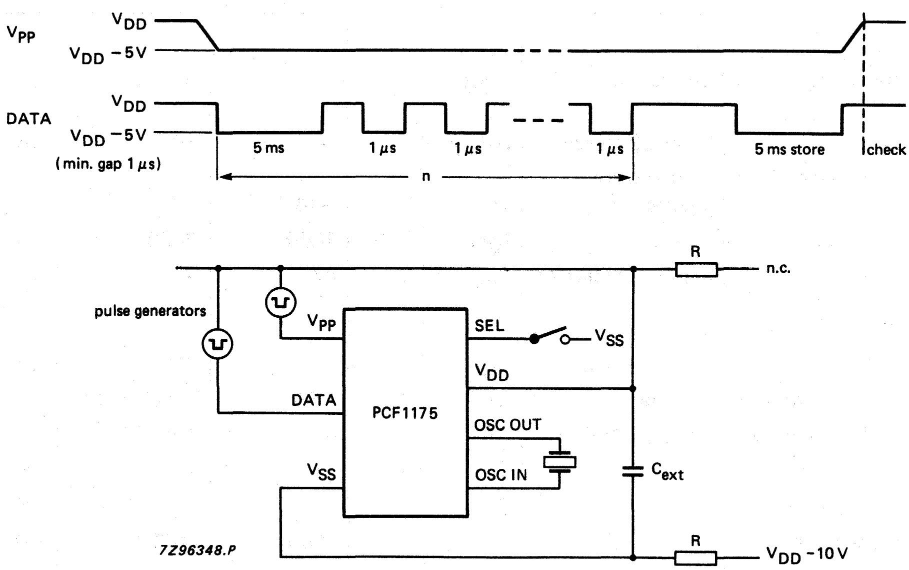


Fig. 6 Programming diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply current (V_{SS} = 0 V); note 1	I_{DD}	max.	3 mA
Voltage range (any pin except V_{PP} and DATA); note 2	V_{I1}		–0,3 to V_{DD} + 0,3 V
Voltage range V_{PP} and DATA	V_{I2}		–3,0 to V_{DD} + 0,3 V
Storage temperature range (unprogrammed)	T_{stg}		–55 to + 125 °C
Operating ambient temperature range	T_{amb}		–40 to + 85 °C

Notes

1. Connecting the supply voltage with reverse polarity will not harm the circuit.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C; crystal: f = 4,194304 MHz, R_s = 50 Ω, C_L = 12 pF; maximum frequency tolerance = ± 30 x 10^{-6}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	programmed	V_{DD}	3	–	6	V
Supply voltage variation	S1 or S2 closed	ΔV_{DD}	–	–	50	mV
Supply voltage	temperature coefficient	TC	–	–16	–	mV/K
Supply current	note 1	I_{DD}	700	1000	2000	µA
Capacitance	external capacitor	C_{ext}	22	47	–	µF
Oscillator						
Start time	$R_{s\,max}$ = 150 Ω	t_{osc}	–	–	200	ms
Frequency deviation	nominal	Δf/f	0	+ 60 x 10^{-6}	+ 120 x 10^{-6}	
Frequency stability	ΔV_{DD} = 100 mV	Δf/f	–	–	1 x 10^{-6}	
Input capacitance		C_i	–	11	–	pF
Output capacitance		C_o	–	24	–	pF
Feedback resistance		R_{fb}	300	1000	3000	kΩ
Inputs	S1, S2, TS, SEL, DATA					
Output current	connected to V_{SS}	I_i	25	–	100	µA
Debounce time	S1 and S2 only	t_d	30	65	100	ms

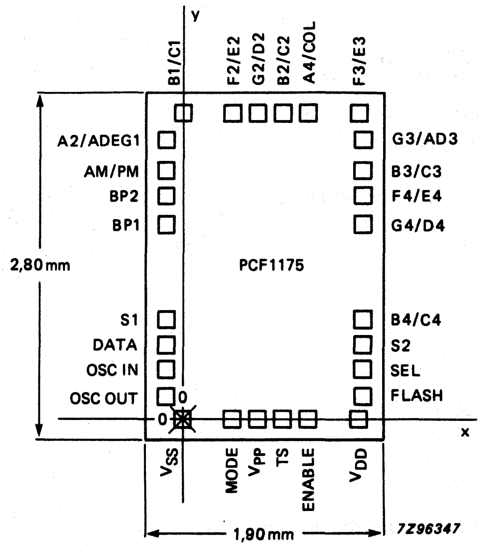
parameter	conditions	symbol	min.	typ.	max.	unit
Input V_{PP}						
Output current	$V_{PP} = V_{DD} -5$ V OSCIN = V_{SS} or V_{DD}	I_{i2}	125	–	500	μA
Output current	during programming	I_{i2}	–	500	–	μA
Backplane	high and low levels					
Output resistance	± 100 μA	R_{bp}	–	–	1	kΩ
Segment						
Output resistance	± 100 μA	R_{seg}	–	–	3	kΩ
LCD						
D.C. offset voltage	200 kΩ/1 nF	V_{dc}	–	–	50	mV

Notes to the characteristics

1. The external resistor R must be chosen appropriately:
   Example: V_{DD} = 5 V, R max. = (12 V – 5 V)/ 700 μA = 10 kΩ
   V_{DD} = 5 V, R typ. = (12 V – 5 V)/1000 μA = 7 kΩ (more reserve).

DEVELOPMENT DATA

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5,32 mm^2
Bonding pad location 100 μm x 100 μm

Fig. 7 Bonding pad locations.

Table 3 Bonding pad dimensions (dimensions in μm)
All x/y co-ordinates are referenced to the bottom left pad (V_{SS}), see Fig. 7.

pad	x	y	pad	x	y
S1	−138	848	G4/D4	1438	1588
DATA	−138	628	F4/E4	1438	1808
OSC IN	−138	408	B3/C3	1438	2028
OSC OUT	−138	188	G3/AD3	1438	2248
V_{SS}	0	0	F3/E3	1400	2476
MODE	400	0	A4/COL	1000	2476
V_{PP}	600	0	B2/C2	800	2476
TS	800	0	G2/D2	600	2476
ENABLE	1000	0	F2/E2	400	2476
V_{DD}	1400	0	B1/C1	0	2476
FLASH	1438	188	A2/ADEG1	−138	2248
SEL	1438	408	AM/PM	−138	2028
S2	1438	628	BP2	−138	1808
B4/C4	1438	838	BP1	−138	1588
chip corner max. value	−300	−160			

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